11-6625-3041-30

ARMY TM 11-6625-3041-30
AIR FORCE TO 33A1-8-908-12

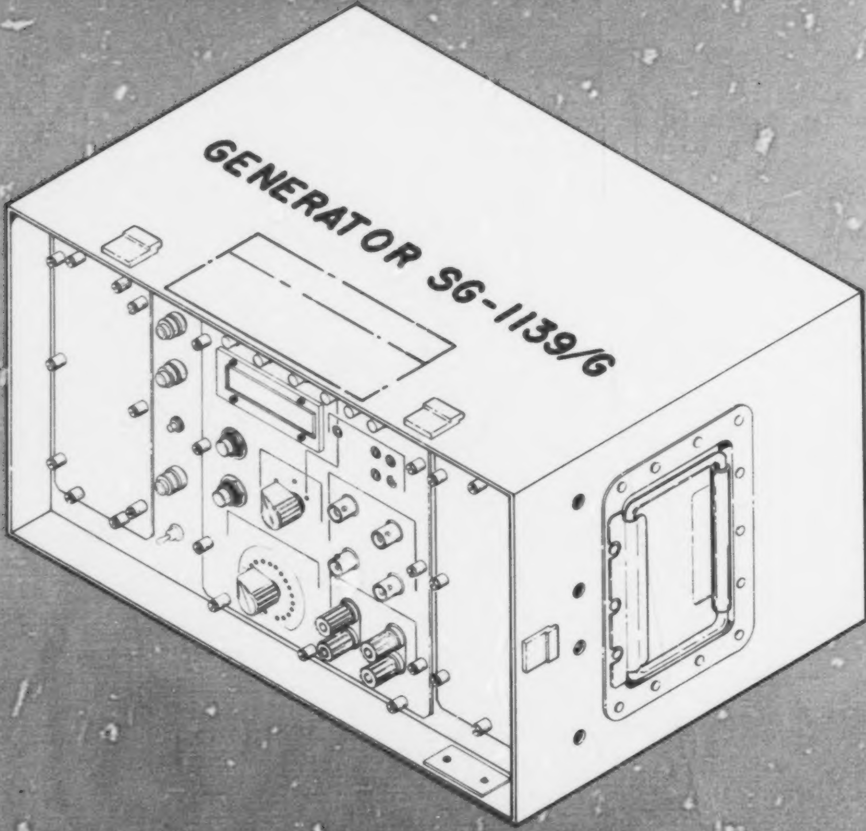
PRINCIPLES OF OPERATION
PAGE 1-5

CHECK PROCEDURES
PAGE 2-3

MAINTENANCE PROCEDURES
PAGE 2-29

FOLDOUTS
FO-1

DIRECT SUPPORT MAINTENANCE MANUAL



DIGITAL DATA GENERATOR

SG-1139/G

(NSN 6625-01-136-2046)

DEPARTMENTS OF THE ARMY AND THE AIR FORCE
7 FEBRUARY 1985

READEX FICHE best copy available

D 101.11:

⑤ SAFETY STEPS TO FOLLOW IF SOMEONE IS THE VICTIM OF ELECTRICAL SHOCK

① DO NOT TRY TO PULL OR GRAB THE INDIVIDUAL

② IF POSSIBLE, TURN OFF THE ELECTRICAL POWER

③ IF YOU CANNOT TURN OFF THE ELECTRICAL POWER, PULL, PUSH, OR LIFT THE PERSON TO SAFETY USING A WOODEN POLE OR A ROPE OR SOME OTHER INSULATING MATERIAL

④ SEND FOR HELP AS SOON AS POSSIBLE

⑤ AFTER THE INJURED PERSON IS FREE OF CONTACT WITH THE SOURCE OF ELECTRICAL SHOCK, MOVE THE PERSON A SHORT DISTANCE AWAY AND IMMEDIATELY START ARTIFICIAL RESUSCITATION

WARNING

HIGH VOLTAGE

The high voltage used in this equipment can kill on contact. Observe the following safety precautions:

• **Ground the Equipment**	Before connecting primary power or the signal cables, connect a heavy gage copper wire from the ground lug on the rear panel to earth ground. Do not remove this wire until the signal cables and primary power have been disconnected.
• **Avoid the Power Input**	Be careful not to contact the 115-volt ac input connections when installing or servicing the equipment.
• **Do Not Service Alone**	Never work on the equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who can administer first aid.
• **Use One Hand**	Where possible, use only one hand to service the equipment. Keep the other hand away to reduce the hazard of current flowing through the vital organs of the body.
• **First Aid**	Be thoroughly familiar with the information contained in FM 21-11 First Aid for Soldiers. Apply first aid to anyone who is the victim of electrical shock.

WARNING

HEAVY EQUIPMENT

This equipment weighs over 35 pounds and can cause serious injury if lifted or carried alone. Observe the following safety precaution:

• **Do Not Lift or Carry Alone**	Do not attempt to lift, carry, or move the equipment by yourself — get help.

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGED PAGES, DESTROY SUPERSEDED PAGES.

NOTE: The portion of the text affected by the changes is indicated by a vertical line in the outer margins of the page. Changes to illustrations are indicated by miniature pointing hands. Changes to wiring diagrams are indicated by shaded areas.

DATES OF ISSUE for original and changed pages are:

Original .. 0 .... 7 February 1985

TOTAL NUMBER OF PAGES in this publication is 152 consisting of the following:

Page No.	Change No.*
Front cover	0
A-C	0
D blank	0
i-iii	0
iv blank	0
1-1 - 1-42	0
2-1 - 2-44	0
A-1	0
A-2 blank	0
B-1 - B-2	0
Gloss-1 - Gloss-2	0
Index-1 - Index-6	0
2028-2 Sample ...	0
2028-2 blanks ...	0
FO-1 - FO-10	0

*Zero in this column indicates an original page.

Technical Manual
TM 11-6625-3041-30
Technical Order
TO 33A1-8-908-12

DEPARTMENTS OF THE ARMY
AND THE AIR FORCE
Washington, DC, 7 February 1985

DIRECT SUPPORT MAINTENANCE MANUAL DIGITAL DATA GENERATOR SG-1139/G (NSN 6625-01-136-2046)

REPORTING ERRORS AND RECOMMENDING IMPROVEMENT

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in the back of the manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5007.

For Air Force, Submit AFTO Form 22 (Technical Order System Publication Improvement Report and Reply) in accordance with paragraph 6-5, Section VI, T.O. 00-5-1. Forward direct to prime ALC/MST activity.

In either case, a reply will be furnished direct to you.

Page

How To Use This Manual iii

Chapter 1 INTRODUCTION

Section I General Information 1-2
II Equipment Description 1-5
III **TECHNICAL PRINCIPLES OF OPERATION** **1-5**

Chapter 2 DIRECT SUPPORT MAINTENANCE

Section I Repair Parts, Special Tools, TMDE, and Support Equipment 2-2
II Service Upon Receipt 2-2
III **EQUIPMENT CHECK PROCEDURES** **2-3**
IV Preventive Maintenance Checks and Services 2-29
V Troubleshooting 2-29
VI **MAINTENANCE PROCEDURES** **2-29**
VII Preparation for Storage or Shipment 2-43

Appendix A References A-1
B Expendable Supplies and Materials List B-1

Glossary Gloss-1
INDEX.......... Index-1

Foldouts

COLOR CODE MARKING (3 Sheets) FO-1
DIGITAL DATA GENERATOR SG-1139/G, Schematic Diagram (3 Sheets) FO-2
A1, MULTI VDC CCA Schematic Diagram (4 Sheets) FO-3
A2, AC INPUT CCA Schematic Diagram (2 Sheets) FO-4
A3, TRANSMIT 1 CCA Schematic Diagram (6 Sheets) FO-5
A4, TRANSMIT 2 CCA Schematic Diagram (6 Sheets) FO-6
A5, RECEIVE 1 CCA Schematic Diagram (7 Sheets) FO-7
A6, RECEIVE 2 CCA Schematic Diagram (4 Sheets) FO-8
A8, CONTROL FILTER ASSEMBLY Schematic Diagram (2 Sheets) FO-9
INTERFACE BOX ASSEMBLY Schematic Diagram FO-10

HOW TO USE THIS MANUAL

Major Subjects	Major subjects are listed on the right side of the front cover and by pages edgemarked in black.
Chapters and Sections	Chapters and sections within the chapters are listed in the overall contents on page i.
Primary Paragraphs	Primary paragraphs (bold-faced headings) for each chapter are listed in the chapter contents at the start of each chapter. Chapters always start on a right-hand page.
Index	An alphabetical index of all subjects starts on page INDEX-1 in the back of the manual.

Chapter 1

INTRODUCTION

CHAPTER CONTENTS

Page

Section I. GENERAL INFORMATION

1-1. Scope 1-2
1-2. Maintenance Forms, Records, and Reports 1-3
1-3. Consolidated Index of Army Publications and Blank Forms 1-3
1-4. Destruction of Army Electronics Materiel to Prevent Enemy Use 1-3
1-5. Reporting Equipment Improvement Recommendations (EIR)............. 1-4
1-6. Administrative Storage 1-4
1-7. Preparation for Storage or Shipment 1-4
1-8. Nomenclature Cross-Reference List 1-4

Section II. EQUIPMENT DESCRIPTION

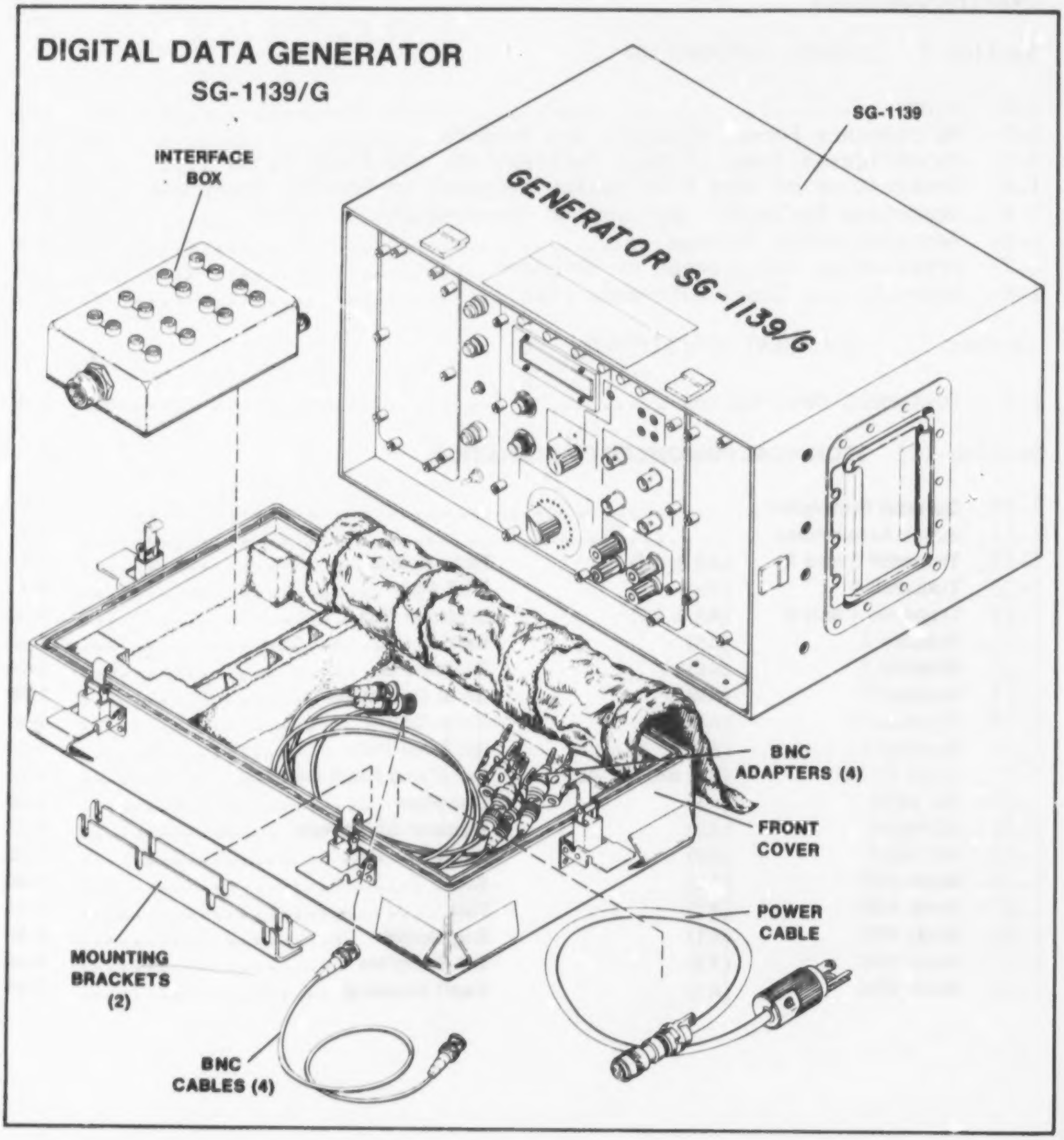
1-9. Equipment Description 1-5

Section III **TECHNICAL PRINCIPLES OF OPERATION**

1-10. **General Principles** **1-5**
1-11. **Major Assemblies** **1-5**
1-12. **Transmit 1 and 2** **(A3 & A4)** **Rate Select** **1-6**
1-13. **Transmit 1** **(A3)** **NRZ Out** **1-7**
1-14. **Transmit 1 and 2** **(A3 & A4)** **Diphase Out** **1-10**
1-15. **Receive 1** **(A5)** **NRZ In** **1-12**
1-16. **Receive 1** **(A5)** **Diphase In** **1-14**
1-17. **Receive 1** **(A5)** **Error Detection** **1-16**
1-18. **Transmit 2** **(A4)** **Error Count** **1-18**
1-19. **Receive 2** **(A6)** **Bit Error Rate** **1-21**
1-20. **Logic Cards** **(A3, A4, A5, A6)** **Input and Fault Sensing** **1-24**
1-21. **AC Input** **(A2)** **Supplies** **1-26**
1-22. **AC Input** **(A2)** **Nuclear Shutdown** **1-27**
1-23. **AC Input** **(A2)** **Fault Sensing** **1-28**
1-24. **Multi VDC** **(A1)** **Start** **1-30**
1-25. **Multi VDC** **(A1)** **Fail** **1-34**
1-26. **Multi VDC** **(A1)** **Regulation** **1-36**
1-27. **Multi VDC** **(A1)** **DC Supplies** **1-40**
1-28. **Multi VDC** **(A1)** **Fault Sensing** **1-41**

Section I

GENERAL INFORMATION



1-1. SCOPE

This manual is for use in maintaining Digital Data Generator SG-1139/G (common name SG-1139). It contains principles of operation and direct support test and repair procedures.

1-2. MAINTENANCE FORMS, RECORDS, AND REPORTS

a. Reports of Maintenance and Unsatisfactory Equipment. Department of the Army forms and procedures used for equipment maintenance will those prescribed by DA Pam 738-750 as contained in Maintenance Management Update. Air Force personnel will use AFR 66-1 for maintenance reporting and TO-00-35D54 for unsatisfactory equipment reporting.

b. Report of Packaging and Handling Deficiencies. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73A/AFR 400-54/MCO 4430.3F.

c. Discrepancy in Shipment Report (DISREP) (SF 361). Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33C/AFR 75-18/MCO P4610.19D/DLAR 4500.15.

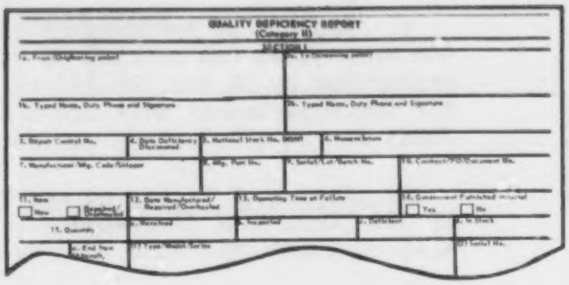
1-3. CONSOLIDATED INDEX OF ARMY PUBLICATIONS AND BLANK FORMS

Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

1-4. DESTRUCTION OF ARMY ELECTRONICS MATERIEL TO PREVENT ENEMY USE

Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2 .

1-5. REPORTING EQUIPMENT IMPROVEMENT RECOMMENDATIONS (EIR)



a. Army. If your Digital Data Generator SG-1139/G needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Put it on an SF 368, Quality Deficiency Report. Mail it to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: AMSEL-ME-MP, Fort Monmouth, New Jersey 07703-5007. We'll send you a reply.

b. Air Force. Air Force personnel are encouraged to submit EIR's in accordance with AFR 900-4.

1-6. ADMINISTRATIVE STORAGE

Administrative storage of equipment issued to and used by Army activities will have preventive maintenance performed in accordance with the PMCS charts before storing. When removing the equipment from administrative storage the PMCS should be performed to assure operational readiness.

1-7. PREPARATION FOR STORAGE OR SHIPMENT

For instructions on preparation for storage or shipment, refer to TM 11-6625-3041-12, Operator's and Organizational Maintenance Manual.

1-8. NOMENCLATURE CROSS REFERENCE LIST

Common Name	Official Nomenclature
SG-1139	Digital Data Generator SG-1139/G
Front cover	Cover assembly, front
Power cable	Cable assembly, power
BNC cable	Cable assembly, coaxial
Mounting bracket	Angle assembly, mounting
BNC adapter	Adapter, BNC-banana
Interface box	Interface assembly
POWER SUPPLY access cover	Cover, front access, power supply
LOGIC access cover	Cover, front access, logic
Multi VDC card	Circuit card assembly, Multi VDC, A1
AC Input card	Circuit card assembly, AC Input, A2
Transmit 1 card	Circuit card assembly, Transmit 1 Board, A3
Transmit 2 card	Circuit card assembly, Transmit 2 Board, A4
Receive 1 card	Circuit card assembly, Receive 1 Board, A5
Receive 2 card	Circuit card assembly, Receive 2 Board, A6
Control filter	Control filter assembly, A8

Section II

EQUIPMENT DESCRIPTION

1-9. EQUIPMENT DESCRIPTION

For equipment description, refer to TM 11-6625-3041-12, Operator's and Organizational Maintenance Manual.

Section III .

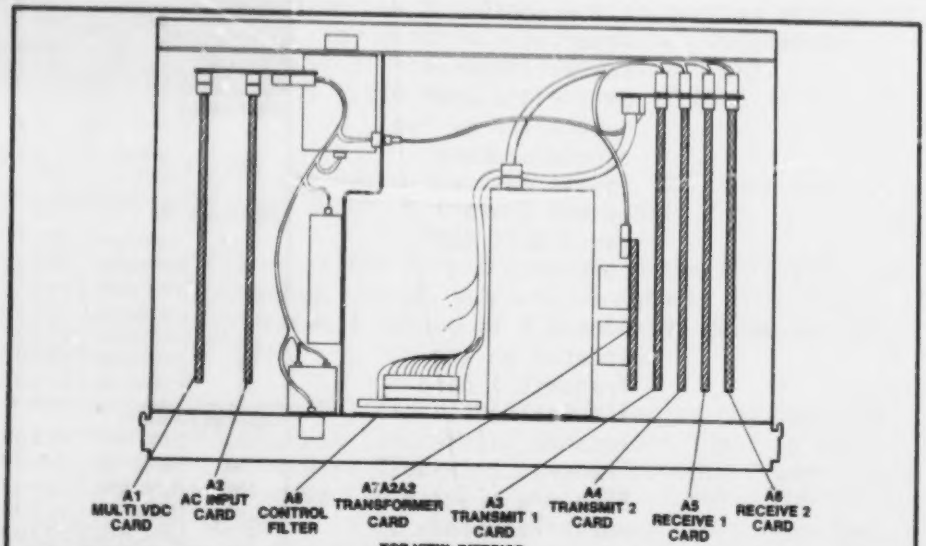
TECHNICAL PRINCIPLES OF OPERATION

1-10. GENERAL PRINCIPLES

For general principles of operation, refer to TM 11-6625-3041-12, Operator's and Organizational Maintenance Manual.

1-11. MAJOR ASSEMBLIES

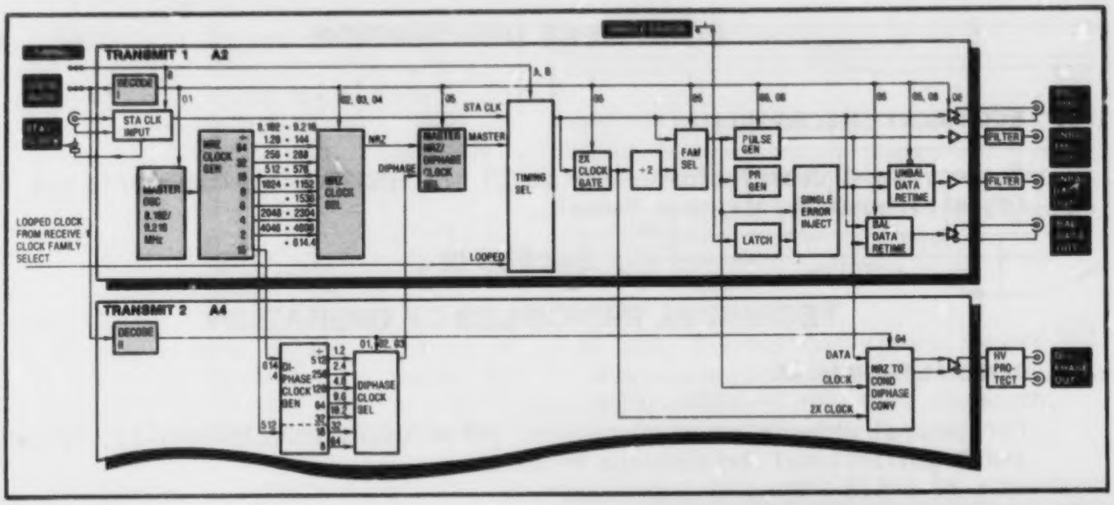
Location



TOP VIEW, INTERIOR

	Assembly	Function	Foldout
Power Supply.	A1 Multi VDC card ...	Switcher .... Dc supplies	F0-3
	A2 AC Input card	Ac rectification .... Switcher supply	F0-4
Logic	A3 Transmit 1 card ..	Clock generation .... Pattern generation NRZ output circuits	F0-5
	A4 Transmit 2 card ..	Diphase output circuits .... Error counting	F0-6
	A5 Receive 1 card ...	Input circuits .... Error detection	F0-7
	A6 Receive 2 card ...	Bit error rate	F0-8
Control	A8 Control Filter ...	Controls, indicators, connectors .	F0-9

1-12. TRANSMIT 1 AND 2 (A3 & A4) RATE SELECT



DATA RATE Control	All circuits associated with the 21 different data rates are controlled by two decoders whose inputs are set by the front panel DATA RATE control.
Decode I, II	Decode I is located on the Transmit 1 card and Decode II is located on the Transmit 2 card. Both are programmable read-only memories (PROMs). The input to each decoder is identical and consists of a 5-bit binary code derived from the DATA RATE control.

The outputs are a set of six or seven binary levels (two outputs from DECODE I and one from DECODE II are not used) that vary with the DATA RATE setting depending on how the PROMs were programmed.

DATA RATE CONTROL SETTING	DATA RATE CONTROL TYPE	DATA RATE CONTROL OUTPUT	DECODE I OUTPUT	DECODE II OUTPUT
576 FAMILY:				
576	UNBAL NRZ	11010	000 100	1110110
.6-32 FAMILY:				
7.6	DIPHASE	00110	011110	0001000
1.2	DIPHASE	10110	011110	1001000
2.4	DIPHASE	~~0111~~0	011110	0101000
4.8	DIPHASE	11110	011110	1101000
9.6	DIPHASE	00001	011110	0011000
16	DIPHASE	10001	111110	1011010
32	DIPHASE	01001	111110	0111010
128-4608 FAMILY:				
128	BAL NRZ	11001	101101	1110010
144	BAL NRZ	00101	001101	1110010
256	BAL NRZ	10101	110101	1110010
288	BAL NRZ	01101	010101	1110010
512	BAL NRZ	11101	100101	1110010
576	BAL NRZ	00011	000101	1110010
1024	BAL NR 2	10011	111001	1110011
1152	BAL NRZ	01011	011001	1110011
1536	BAL NRZ	11011	001001	1110011
2048	BAL NRZ	00111	110001	1110011
2304	BAL NRZ	10111	010001	1110011
4096	BAL NRZ	01111	100001	1110011
4608	BAL NRZ	11111	000001	1110011

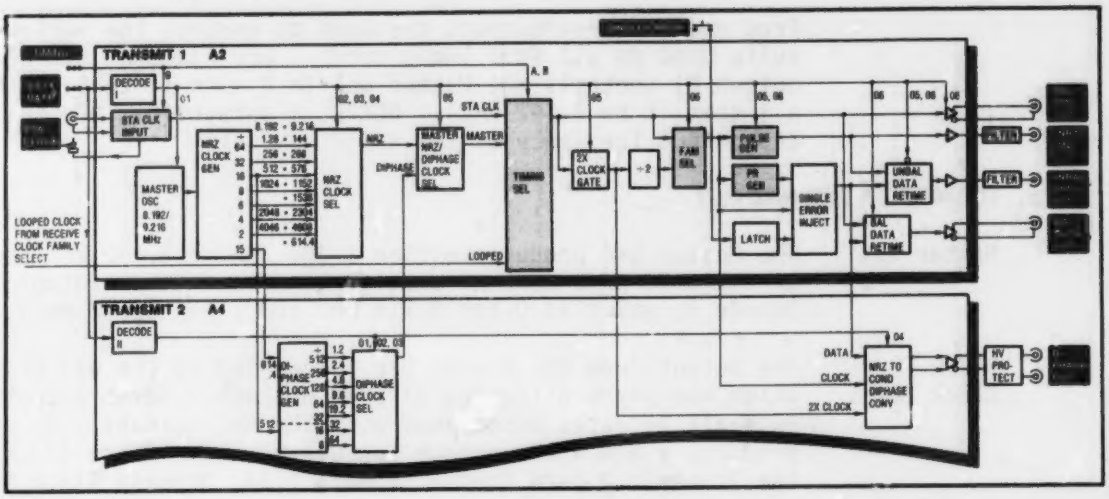
1-12. TRANSMIT 1 AND 2 (A3 & A4) RATE SELECT (CONT)

From one to three outputs are used to control the various circuits used on all four logic cards. For example, DECODE I output 01 controls the Master Osc (a 0 sets it to 9.216 MHz and a 1 sets it to 8.192 MHz). DECODE I outputs 01, 02, and 03 set the output frequency of the NRZ Clock Sel.

1-13. TRANSMIT 1 (A3) NRZ OUT

Master Osc	The Master Osc produces either 9.216 MHz or 8.192 MHz depending on the DATA RATE control setting (through the 01 output from Decode I, which is 0 for 9.216 MHz and 1 for 8.192 MHz).
NRZ Clock Gen	The output from the Master Osc is applied to the NRZ Clock Gen, which has eight different divider outputs. Seven outputs produce all 13 rates associated with the NRZ outputs. An eighth produces a 614.4 kHz output for use by the Diphase Clock Gen on the Transmit 2 card (refer to para 1-14, Diphase Clock Gen). The actual output from the NRZ Clock Gen depends on the output of the Master Osc. For example, if the Master Osc output is 8.192 MHz, the output of the ÷64 divider is 128 kHz. If the Master Osc output is 9.216 MHz, the output of the ÷64 divider is 144 kHz.
NRZ Clock Sel	The outputs from the seven dividers in the NRZ Clock Gen are applied to the input of the NRZ Clock Sel. The input selected as the output depends on the DATA RATE control setting (through the 02, 03, and 04 outputs from Decode I). For example, a Decode I output of 011 sets the NRZ Clock Sel output to 128 kHz.
Master NRZ/ Diphase Clock Sel	The output from the NRZ Clock Sel is applied as one input to the Master NRZ/Diphase Clock Sel. The second input is the output from the Diphase Clock Sel on the Transmit 2 card (refer to para 1-14, Diphase Clock Sel). For NRZ signals, the 05 output from Decode I is 0, which selects the input from the NRZ Clock Sel as the output from the Master NRZ/Diphase Clock Sel.

1-13. TRANSMIT 1 (A3) NRZ OUT (CONT)



TIMING Control All transmit circuits associated with the three different timing sources are controlled by the front panel TIMING control. The output from this control is a 2-bit binary code that determines the timing source as follows:

TIMING Control

	Setting	Output Code A	Output Code B	
	LOOPED	0	1	Transmit timing is derived from signals applied to receiver input (refer to para 1-15, Clock Fam Sel).
STA CLK Input	STA CLK	1	0	Transmit timing is derived from external signal applied to the front panel STA CLK input connector. In this timing mode, a front panel indicator lights when a signal is applied to the connector.
	MASTER	1	1	Transmit timing is derived from the Master Osc.

Timing Sel All three timing signals (Sta Clk, Looped, and Master) are applied to the Timing Sel. Depending on the setting of the TIMING control, one of the inputs is selected as the output.

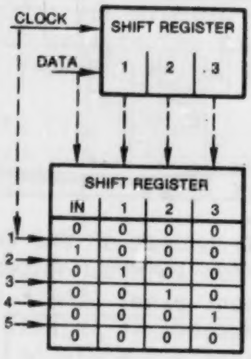
BALANCED TMG OUT The output from the Timing Sel is applied to an amplifier, converted to a balanced (2-wire) output, and applied to the front panel BALANCED TMG OUT connector. The 1-level 06 output from Decode I enables this amplifier only for the 126-4608 family of DATA RATES (balanced NRZ).

Fam Sel The output from the Timing Sel is also applied to the input of the Fam Sel. A 0-level 05 output from Decode I (576 family of DATA RATES) selects this input as the output from the Fam Sel.

1-13. TRANSMIT 1 (A3) NRZ OUT (CONT)

Pulse Gen	The input from the Fam Sel is applied to the Pulse Gen, which converts the symmetrical input to 120-ns wide pulses.
UNBALANCED TMG OUT	The output from the Pulse Gen is applied to an amplifier and through a filter to the front panel UNBALANCED TMG OUT connector.
PR Gen	The output of the Fam Sel is also applied to the clock input of the PR (pseudorandom) Gen, which consists of a shift register with feedback.

Upon application of a clock pulse, an input value is accepted into the first shift register stage. With each succeeding clock pulse, the input value is shifted to the next stage. With no new input value, the clock pulses will eventually clear the register.



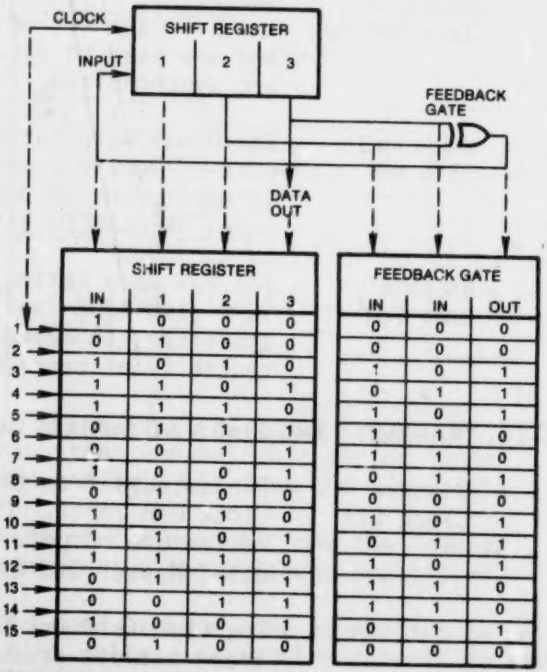
SHIFT REGISTER

	IN	1	2	3
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	0	0	1	0
5	0	0	0	1
	0	0	0	0

In a pseudorandom generator, a feedback path containing a 2-input exclusive-OR gate is added to the shift register. The inputs to the gate are taken from two stages of the shift register, and the output is fed back to the input of the register.

The resultant data signal out is a repeating binary sequence of ones and zeros.

In the SG-1139 there are 15 stages in the shift register, which produce a pattern of 32,767 bits. This pattern is long enough so that the system under test responds as if the sequence was truly random.



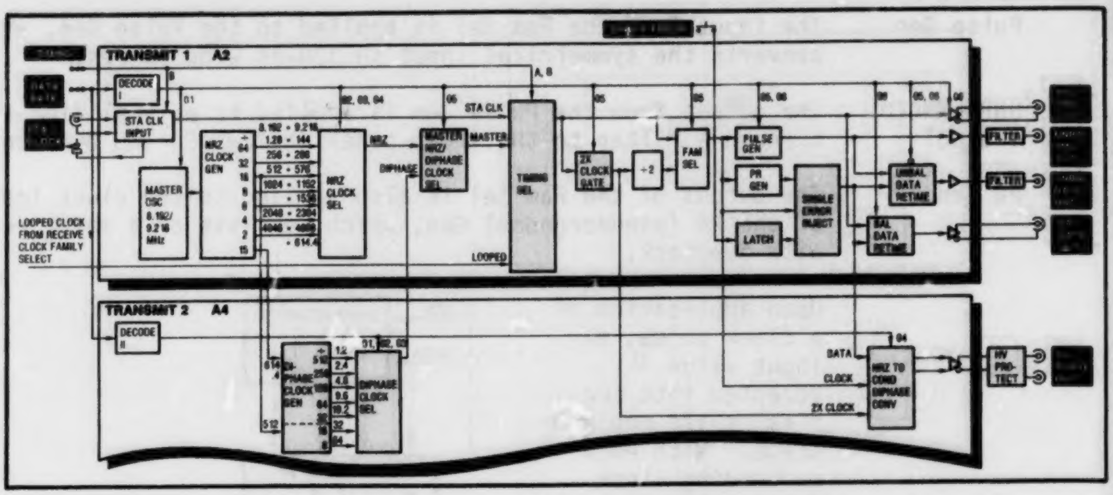
SHIFT REGISTER

	IN	1	2	3
1	1	0	0	0
2	0	1	0	0
3	1	0	1	0
4	1	1	0	1
5	1	1	1	0
6	0	1	1	1
7	0	0	1	1
8	1	0	0	1
9	0	1	0	0
10	1	0	1	0
11	1	1	0	1
12	1	1	1	0
13	0	1	1	1
14	0	0	1	1
15	1	0	0	1
	0	1	0	0

FEEDBACK GATE

IN	IN	OUT
0	0	0
0	0	0
1	0	1
0	1	1
1	0	1
1	1	0
1	1	0
0	1	1
0	0	0
1	0	1
0	1	1
1	0	1
1	1	0
1	1	0
0	1	1
0	0	0

1-13. **TRANSMIT 1 (A3) NRZ OUT** (CONT)



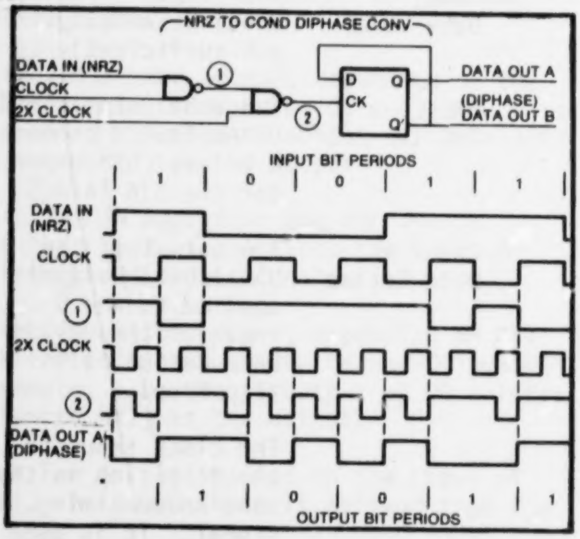
Single Error Inject	The output of the PR Gen is applied to the input of the Single Error Inject. A second input is from a latch activated by the front panel SINGLE ERROR pushbutton. Each time the button is pressed, it injects an error (a 0 where a 1 would be or a 1 where a 0 would be).
Unbal/Bal Data Retime	The output of the Single Error Inject is applied to the Unbal and Bal Data Retime circuits. Both operate in the same manner and are used to ensure the timing outputs and data outputs are synchronized.
UNBALANCED DATA OUT	The Unbal Data Retime is enabled when both the 05 and 06 outputs of Decode I are 0 (576 family DATA RATE). Its output is applied to an amplifier and through a filter to the front panel UNBALANCED DATA OUT connector.
BALANCED DATA OUT	The Bal Data Retime is enabled when the 06 output of Decode I is 1 (128-4608 family DATA RATE). Its output is applied to an amplifier, converted to a balanced (2-wire) output, and applied to the front panel BALANCED DATA OUT connector.

1-14. **TRANSMIT 1 AND 2 (A3 & A4) DIPHASE OUT**

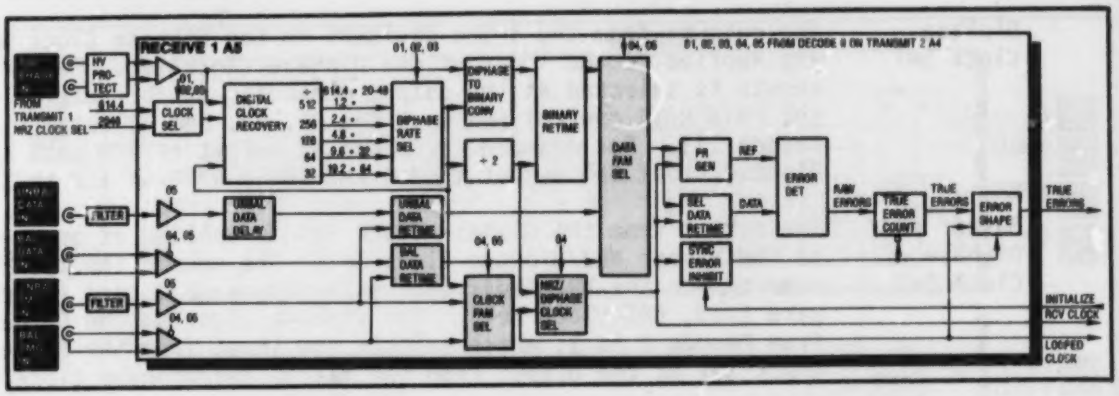
Diphase Clock Gen	Two outputs from the NRZ Clock Gen are applied to the Diphase Clock Gen input. One is 614.4 kHz derived from the 9.216 MHz Master Osc output. The other is 512 kHz derived from the 8.192 Master Osc output. The Diphase Clock Gen has seven different divider outputs. These outputs produce the seven rates associated with diphase outputs. Each rate is twice the actual diphase DATA RATE setting because two transitions are required for each logic 0 bit, one a half-bit later than the other.

1-14. TRANSMIT 1 AND 2 (A3 & A4) DIPHASE OUT (CONT)

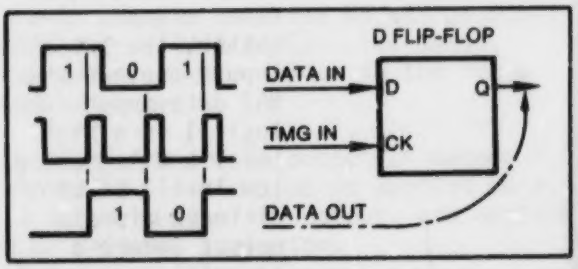
Diphase Clock Sel	The outputs from the seven dividers in the Diphase Clock Gen are applied to the input of the Diphase Clock Sel. One of the inputs is selected as the output depending on the setting of the DATA RATE control (through the 01, 02, and 03 outputs from Decode II). For example, a Decode II output of 100 sets the Diphase Clock Sel output to 2.4 kHz (DATA RATE of 1.2 kb/s).
Master NRZ/ Diphase Clock Sel	The output from the Diphase Clock Sel is applied as one input to the Master NRZ/Diphase Clock Sel. The second input is the output from the NRZ Clock Sel on the Transmit 2 card (refer to para 1-13, NRZ Clock Sel). For diphase signals, the 05 output from Decode I is 1, which selects the input from the Diphase Clock Sel as the output from the Master NRZ/Diphase Clock Sel.
Timing Sel	Three timing signals (Sta Clk, Looped, and Master) are applied to the Timing Sel. Depending on the setting of the TIMING control, one of the inputs is selected as the output.
2X Clock Gate	The output of the Timing Sel is applied to the input of the 2X Clock Gate. The 2X Clock Gate is enabled by the 1-level 05 output from Decode I.
NRZ to Cond Diphase Conv	The output from the 2X Clock Gate is applied as one clock input to the NRZ to Cond Diphase Conv. The second clock input is the normal Clock signal. Together, the two clock inputs convert the NRZ data input (where logic 1 is a high level and logic 0 a low level) to conditioned diphase output (where a transition occurs for every bit period and a logic 0 is a second transition one-half bit period later). The output data is shifted one-half bit from the input data. The Diphase output consists of two outputs, one the inverse of the other. These outputs drive the balanced amplifiers.
DIPHASE OUT	The output from the NRZ to Cond Diphase Conv is applied to an amplifier and through a high-voltage protection circuit to the DIPHASE OUT connectors.



1-15. RECEIVE 1 (A5) NRZ IN

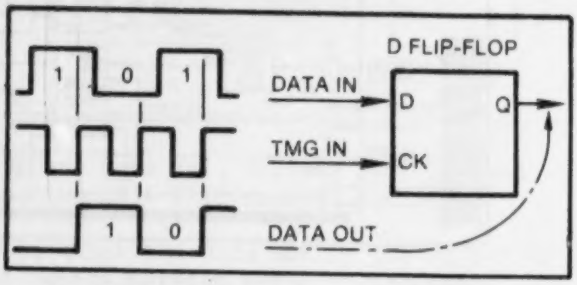


UNBAL DATA IN	The unbalanced data signal is applied to the front panel UNBALANCED DATA IN connector, through a filter, and to an amplifier. A 1-level 05 output from Decode II enables the amplifier only for the 576 (ATACS) family DATA RATE (unbalanced NRZ).
Unbal Data Delay	The output from the amplifier is applied to the input of the Unbal Data Delay. The Unbal Data Delay delays the data input sufficiently to ensure it lags the timing input.
UNBAL TMG IN	The unbalanced timing signal is applied to the front panel UNBAL TMG IN connector, through a filter, and to an amplifier. A 1-level 05 output from Decode II enables the amplifier only for the 576 (ATACS) family DATA RATE (unbalanced NRZ).
Unbal Data Retime	The output of the Unbal Data Delay is applied to the D input of the Unbal Data Retime, a D flip-flop. The clock input to the flip-flop is the unbalanced timing signal. It is used to clock the data out of the flip-flop to ensure the data input is in phase with the timing input.
BAL DATA IN	The balanced data signal is applied to the front panel BALANCED DATA IN connector and to an amplifier. A 0-level 04 and a 0-level 05 output from Decode II enable the amplifier only for the 128-4608 family DATA RATES (balanced NRZ).

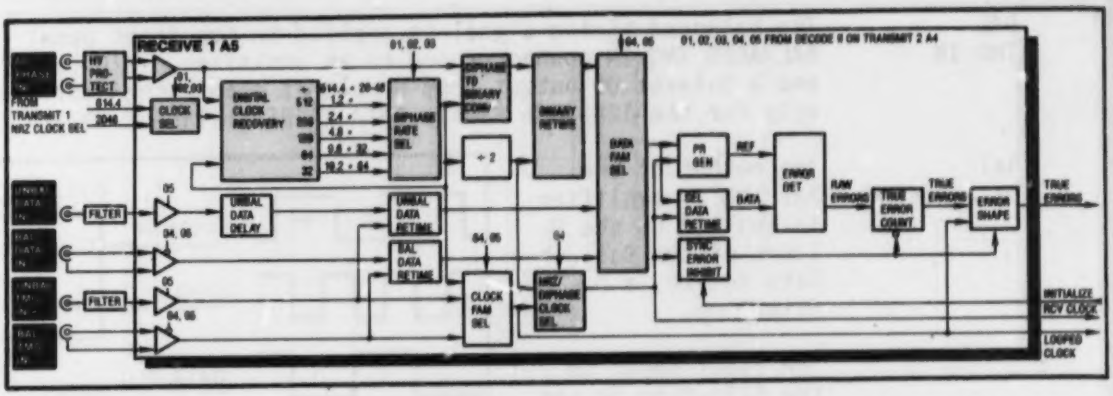


1-15. RECEIVE 1 (A5) NRZ IN (CONT)

BAL TMG IN	The balanced timing signal is applied to the front panel BALANCED TMG IN connector and to an amplifier. A 0-level 04 and a 0-level 05 output from Decode II enable the amplifier only for the 128-4608 family DATA RATES (balanced NRZ).
Bal Data Retime	The output of the BAL TMG IN amplifier is applied to the D input of the Bal Data Retime, a D flip-flop. The clock input to the flip-flop is the balanced timing signal. It is used to clock the data out of the flip-flop (in the same manner as the Unbal Data Retime above) to ensure the data input is in phase with the timing input.
Data Fam Sel	The outputs from the Unbal Data Retime and Bal Data Retime are applied to the input of the Data Fam Sel. A third input is derived from the diphase signal. One of the inputs is selected as the output, depending on the setting of the DATA RATE control (through the 04 and 05 outputs from Decode II). For example, a Decode II output of 00 selects the 128-4608 family (balanced NRZ) as the output.
Clock Fam Sel	The output from the UNBAL TMG IN amplifier and BAL TMG IN amplifier are applied to the input of the Clock Fam Sel. A third input is derived from the diphase signal. One of the inputs is selected as the output, depending on the setting of the DATA RATE control (through the 04 and 05 outputs from Decode II). For example, a Decode II output of 00 selects the 128-4608 family (balanced NRZ) as the output.
NRZ/Diphase Clock Sel	The output from the Clock Fam Sel is applied to the input of the NRZ/Diphase Clock Sel. A second input is derived from the diphase signal. One of the inputs is selected as the output, depending on the setting of the DATA RATE control (through the 04 output from Decode II). For example, a Decode II output of 0 selects the 576 ATACS or 128-4608 family (NRZ) as the output.



1-16. RECEIVE 1 (A5) DIPHASE IN

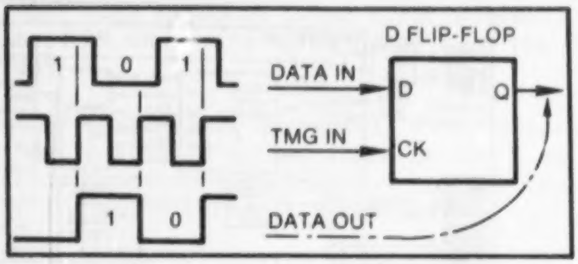


DIPHASE IN	The diphase signal is applied to the front panel DIPHASE IN connector, through a high-voltage protection circuit, to an amplifier.
Clock Sel	The inputs to the Clock Sel are 614.4 kHz and 2048 kHz from the NRZ Clock Sel on the Transmit 1 card. The 614.4 kHz input is selected as the output by the DATA RATE control for the first five settings (.6-9.6) through the 01, 02, and 03 outputs of the Decode II. The 2048 kHz input is selected as the output for the last two settings (16 and 32).
Digital Clock Recover	The data output from the DIPHASE IN amplifier and the clock output from the Clock Sel are applied to the Digital Clock Recovery. The Digital Clock Recovery has five different divider outputs. The actual output of the Digital Clock Recovery depends on the output of the Clock Sel. For example, if the Clock Sel has been set for 2048 kHz, the output of the ÷64 divider will be 32 kHz. Each rate is twice the actual diphase DATA RATE setting because two transitions are required for each logic 0 bit, one a half-bit later than the other.
Diphase Rate Sel	The outputs from the five dividers in the Digital Clock Recovery are applied to the input of the Diphase Rate Sel. The input selected as the output depends on the setting of the DATA RATE control (through the Q1, Q2, and Q3 outputs from Decode II). For example, a Decode II output of 101 sets the Diphase Rate Sel to 32 kHz, corresponding to a DATA RATE setting of 16 kb/s.
Diphase to Binary Conv	The data output from the DIPHASE IN amplifier and the clock output from the Diphase Rate Sel are applied to the input of the Diphase to Binary Conv. The Diphase to Binary Conv converts diphase data to binary data.

1-16. RECEIVE 1 (A5) DIPHASE IN (CONT)

Binary Retime

The data output of the Diphase to Binary Conv is applied to the D input of the Binary Retime, a D flip-flop.



The clock input to the flip-flop is the clock output from the Diphase Rate Sel, divided by 2 so that it is at the same rate as the DATA RATE control setting.

The clock input is used to clock the data out of the flip-flop to ensure the data input is in phase with the timing input.

Data Fam Sel

The output from the Binary Retime is applied to the input of the Data Fam Sel. Two other inputs are from the Unbal and Bal Data Retime.

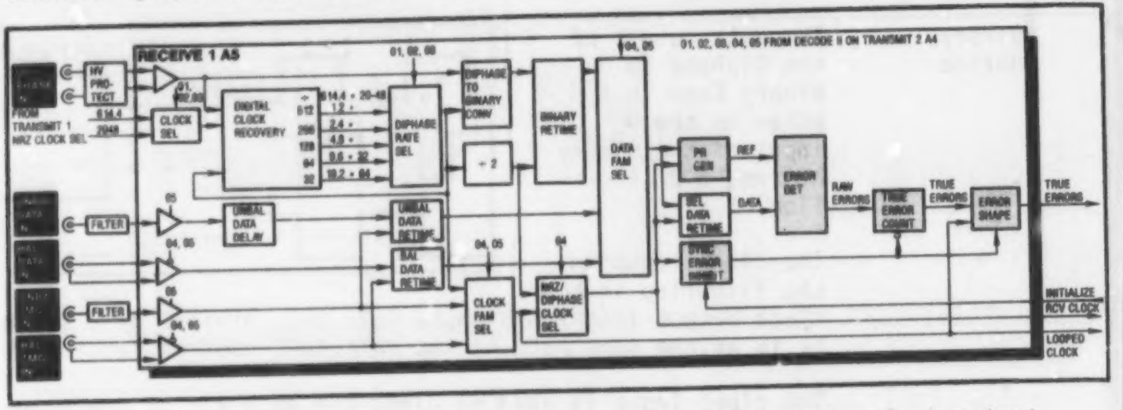
One of the inputs is selected as the output, depending on the setting of the DATA RATE control (through the 04 and 05 outputs from Decode II). For example, a Decode II output of 10 selects the .6-32 family (diphase) as the output.

NRZ/Diphase Clock Sel

The clock output from the Diphase Rate Sel, divided by 2, is applied to the NRZ/Diphase Clock Sel. A second input is the NRZ clock signal from the Clock Fam Sel.

One of the inputs is selected as the output, depending on the setting of the DATA RATE control (through the 04 output from Decode II). For example, a Decode II output of 1 selects the .6-32 family (diphase) as the output.

1-17. RECEIVE 1 (A5) ERROR DETECTION

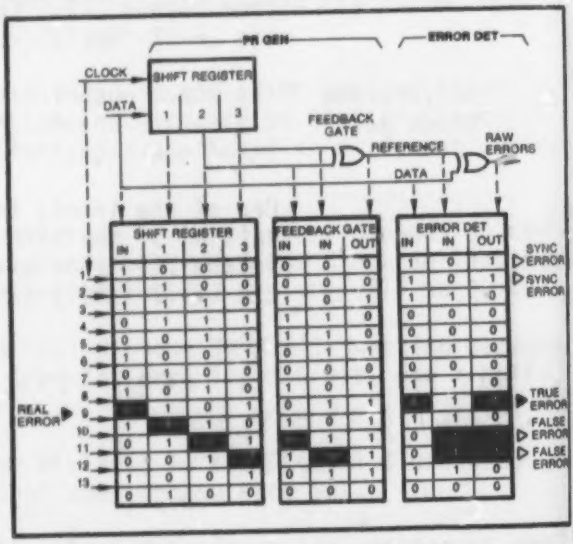


PR Gen The data output from the Data Fam Sel and the clock output from the NRZ/Diphase Clock Sel are applied to the PR Gen. This PR Gen is identical to the one used on the Transmit 1 card for data output (refer to para 1-13, PR Gen).

The clock input shifts the data input through the shift register in the PR Gen. The outputs of the register are applied to a feedback gate, which is an exclusive-OR gate.

Error Det The output of the feedback gate in the PR Gen is applied to one input of the Error Det, which is another exclusive-OR gate.

The second input to the Error Det is the data output from the Data Fam Sel through the Sel Data Retime.



SHIFT REGISTER			
IN	1	2	3
1	0	0	0
1	1	0	0
1	1	1	0
0	1	1	1
0	0	1	1
1	0	0	1
0	1	0	0
1	0	1	0
[illegible]	1	0	1
1	[illegible]	1	0
0	1	[illegible]	1
0	0	1	[illegible]
1	0	0	1
0	1	0	0

FEEDBACK GATE		
IN	IN	OUT
0	0	0
0	0	0
1	0	1
1	1	0
1	1	0
0	1	1
0	0	0
1	0	1
0	1	1
1	0	1
[illegible]	1	1
1	[illegible]	1
0	1	1
0	0	0

ERROR DET		
IN	IN	OUT
1	0	1
1	0	1
1	1	0
0	0	0
0	0	0
1	1	0
0	0	0
1	1	0
[illegible]	1	[illegible]
1	1	0
0	[illegible]	[illegible]
0	1	[illegible]
1	1	0
0	0	0

After a number of consecutive error-free data bits corresponding to the number of stages in the shift register (3 in the example, 15 in the SG-1139), the register will begin to output the same data pattern as the input (the PR Gen is synchronized).

Whenever the input from the Data Fam Sel (data) differs from that of the PR Gen (reference), the Error Det produces an outpu

(raw errors).

1-17. RECEIVE 1 (A5) ERROR DETECTION (CONT)

True Error Count

Each real error in the input data produces three error pulses in the Error Det output because there are three paths from the data input to the error output.

To prevent an error count of three times the actual input errors, the output of the Error Det is applied to the input of the True Error Count. The True Error Count is a divide-by-3 counter that produces one output pulse for every three it receives.

Error Shape

The output of the True Error Count is applied to the input of the Error Shape.

The true errors output from the Error Shape is applied to the ERRORS counter and BER indicator circuits on the Receive 2 card.

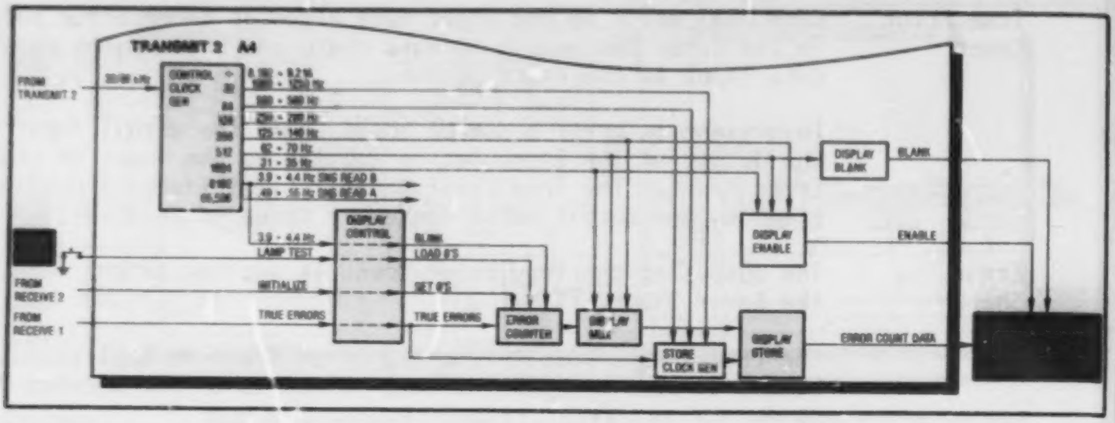
Sync Error Inhibit

Before the PR Gen is synchronized to the input data, the Error Det will produce a number of error pulses up to one less than the number of stages in the shift register (2 in the example, 14 in the SG-1139).

To prevent an error count during the synchronization process, a Sync Error Inhibit is used. The Sync Error Inhibit is a divide-by-16 counter that is driven by the clock output from the NRZ/Diphase Clock Sel. It is set to zero (initialized) by a signal from the Receive 2 card (refer to para 1-19, BER control) which occurs when power is first applied, when timing inputs are first applied, or when the RESET button is pushed, etc.

During the time the first 16 clock pulses are applied, after initialization, the output from the Sync Error Inhibit prevents operation of the True Error Count and Error Shape so that sync errors are not counted.

1-18. TRANSMIT 2 (A4) ERROR COUNT



Control Clock Gen The divide-by-16 output (32/36 kHz) from the Diphase Clock Gen on the Transmit 2 card (para 1-14, Diphase Clock Gen) is applied to the input of the Control Clock Gen.

The Control Clock Gen has eight different divider outputs. Each output can be one of two different rates, depending on whether the DATA RATE control has set the Master Osc for an output of 8.192 or 9.216 MHz.

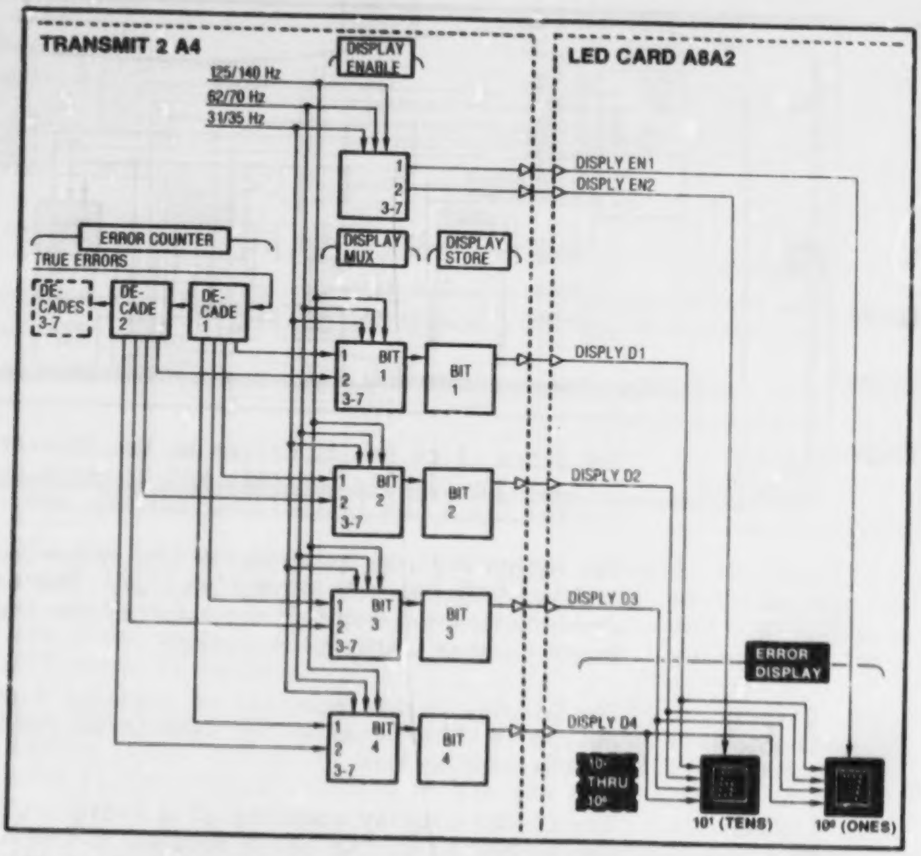
Display Control The 3.9/4.4 Hz output from the Control Clock Gen is applied through the Display Control as a blink input to the Error Counter.

When the front panel LAMP TEST pushbutton is pressed, the 0-level signal is applied through the Display Control as a Load input to the Error Counter. This loads an 8 into each of its 7-decade dividers.

The initialize signal from the BER Control on the Receive 2 card is applied through the Display Control as a clear input to the Error Counter, which sets a 0 into each of its 7-decade counters.

The true errors signal from the Error Shape on the Receive 1 card is applied through the Display Control to the input of the Error Counter, which advances its count by one each time a true-errors pulse is received.

1-18. TRANSMIT 2 (A4) ERROR COUNT (CONT)



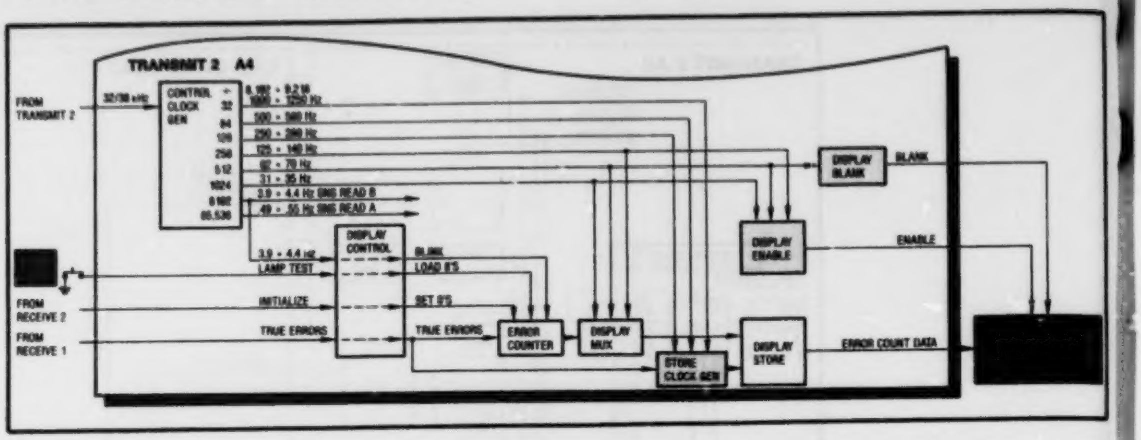
Error Counter The Error Counter consists of seven decades, each with a 4-bit BCD output. Each bit from each decade is applied to the input of the Display Mux.

Display Mux The Display Mux consists of four 1-of-7 selectors, one selector for each bit from the decades in the Error Counter. The inputs to the selectors are the 4-bit outputs from the decades in the Error Counter.

The input selected as the output is determined by three outputs from the Control Clock Gen (125/140, 62/70, and 31/35 Hz). These inputs sequentially select the four bits from decade 1, 2, 3, etc., as the output.

Display Store The 4-bit output from the Display Mux is applied to the Display Store. The Display Store stores each bit briefly and provides current drive for the LEDs in the display.

1-18. TRANSMIT 2 (A4) ERROR COUNT (CONT)



Store Clock Gen The Store Clock Gen is driven by the true-errors signal through the Display Control, and by three outputs from the Control Clock Gen (1000/1250, 500/560, and 250/280 Hz).

Its output is used to transfer the error-count data in the Display Store to the ERRORS display. The true-errors input prevents the transfer of data during the time the count in the Error Counter would be changing.

Display Enable The Display Enable consists of a single 1-of-7 selector whose output is determined by the same three inputs as the selectors in the Display Mux.

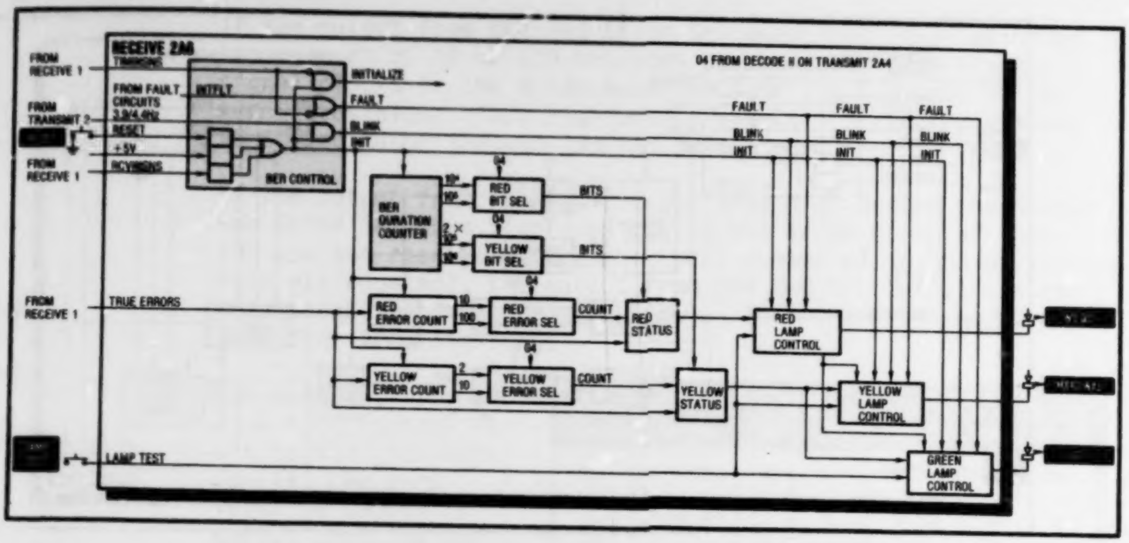
ERRORS Displays The ERRORS display consists of a 7-digit LED display corresponding to the seven decades in the Error Counter. The 4-bit error-count data from the Display Store is applied to all seven display digits.

The enable signals from the Display Enable allow only one display digit at a time to accept the error-count data. The digit selected corresponds to the decade selected in the Error Counter. Since both the Display Mux and Display Enable are driven by the same three clock signals, the decade selected for output and the digit selected for input are identical.

In this way, the 28-line data (7 decades x 4 bits) is reduced to 11-line data (7 enable signals + 4 bits) in order to minimize wiring.

Display Blank The 62/70 Hz output from the Control Clock Gen is applied to the Display Blank. Its output is applied to the ERRORS display and is used to blank the display at a 62 to 70 Hz rate in order to minimize power consumption.

1-19. RECEIVE 2 (A6) BIT ERROR RATE



BER Control

The BER Control produces an Init output whenever the front panel RESET button is pressed (Reset output), when the unit is first turned on (+5V input), or when the data and timing inputs are first applied (Rcvinsns input). The Init output sets the BER circuits to zero.

The BER Control produces an Initialize output whenever the timing input is missing (Timinsns). The Initialize output is used by the Transmit 2 card to set the Error Counter to zero.

The BER Control produces a Fault output whenever the timing input is missing (Timinsns) or a fault is sensed (Intflt, refer to para 1-20). The Fault output turns off all three BER indicators.

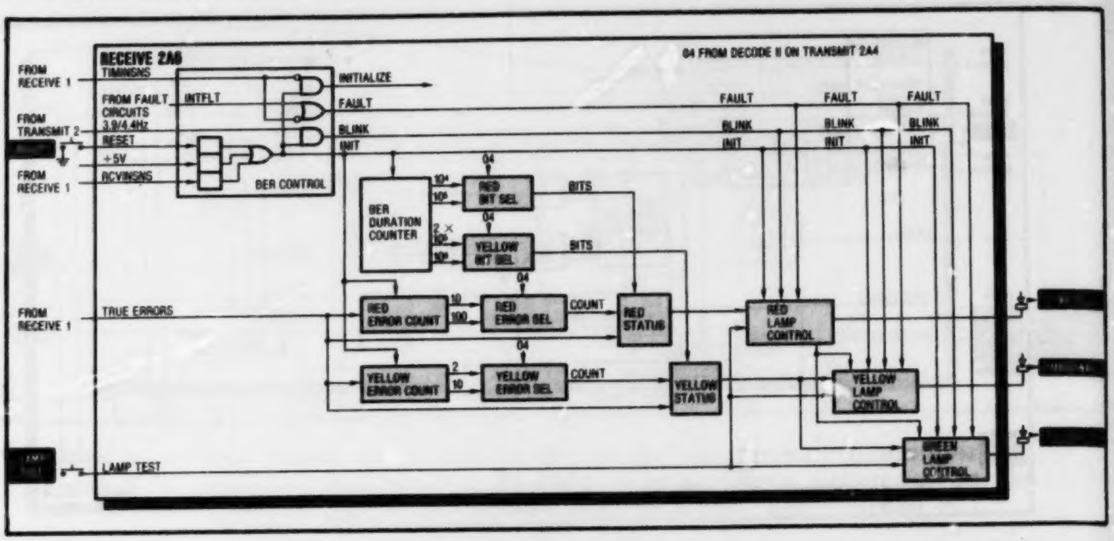
The BER Control produces a blink output during the initialization period. The Init output allows the 3.9/4.4 Hz output from the Control Clock Gen on the Transmit 2 card (para 1-18, Control Clock Gen) to pass through the gate and cause the BER lamps to blink on and off approximately four times a second.

BER Duration Counter

The BER Duration Counter accepts the Revclock input pulses from the NRZ/Diphase Clock Sel on the Receive 1 card (para 1-15, NRZ/Diphase Clock Sel) and counts the pulses, which represent the number of data bits received.

The counter produces four outputs: one after 10,000 bits have been counted (10^4), one after 100,000 bits (10^5), one after 200,000 bits (2×10^5), and one after 1,000,000 bits (10^6).

1-19. RECEIVE 2 (A6) BIT ERROR RATE (CONT)



Red Bit Sel

The 10^4 and 10^5 outputs from the BER Duration Counter are applied to the Red Bit Sel. The input selected for output depends on the setting of the front panel DATA RATE control through the 04 output from Decode II on the Transmit 2 card (refer to para 1-12, DATA RATE Control). A setting for the 576 or 128-4608 families causes an 04 output to zero, which selects the 10^5 input as the output. A setting for the .6-32 family causes an 04 output of 1, which selects the 10^4 input.

Red Error Count

True errors from the Error Shape on the Receive 1 card (refer to para 1-17, Error Shape) are applied to the Red Error Count, which counts the errors.

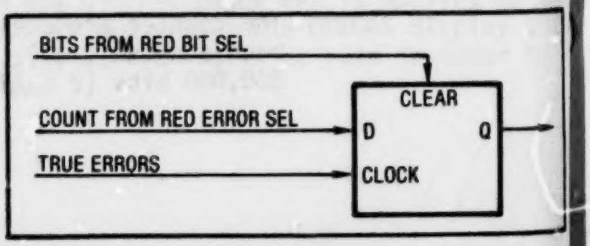
The counter produces two outputs: one after 10 errors have been counted (10) and one after 100 errors have been counted (100).

Red Error Sel

The 10 and 100 outputs from the Red Error Count are applied to the Red Error Sel. The input selected for output depends on the setting of the front panel DATA RATE control through the 04 output from Decode II on the Transmit 2 card (refer to para 1-12, DATA RATE control). A setting for the 576 or 128-4608 families causes an 04 output of zero, which selects the 100 input as the output. A setting for the .6-32 family causes an 04 output of 1, which selects the 10 input.

Red Status

The Red Status is a data flip-flop whose D input is the output from the Red Error Sel.



-19. RECEIVE 2 (A6) BIT ERROR RATE (CONT)

If the output from the Red Error Sel goes high (indicating an error count of 10 or 100 has been reached) the true errors signal clocks in the D input, which sets the Q output of the Red Status high. This high output lights the red front panel NO GO indicator through the Red Lamp Control.

If the output from the Red Bit Sel goes high before the output Red Error Sel goes high (indicating the error count of 10 or 100 was not reached before the total number of 10,000 or 100,000 bits was counted), the output from the Red Bit Sel clears the Red Status (sets its Q output low). This prevents the NO GO indicator from lighting.

For example, if the DATA RATE control is set to 512 (128-4608 family) the zero level 04 Decode II output sets the Red Error Sel for the 100 output and the Red Bit Sel for the 10^5 output (100 errors per 100,000 bits).

DATA RATE FAMILY	YELLOW CONTROL			RED CONTROL		
	BITS	TIME	COUNT	BITS	TIME	COUNT
576	1,000,000	1.7s	10	100,000	.17s	100
6–32	200,000	5.6m to 6.3s	2	10,000	34s to .63s	10
128–4608	1,000,000	7.8s to .2s	10	100,000	.78s to .02s	100

If 100 errors are counted before 100,000 bits have been counted, the red NO GO indicator lights.

Red Lamp Control The output from the Red Status is applied to the Red Lamp Control, which includes a driver to light the NO GO indicator. It also includes a latch so that the results from one BER measurement can be indicated while another measurement is in progress.

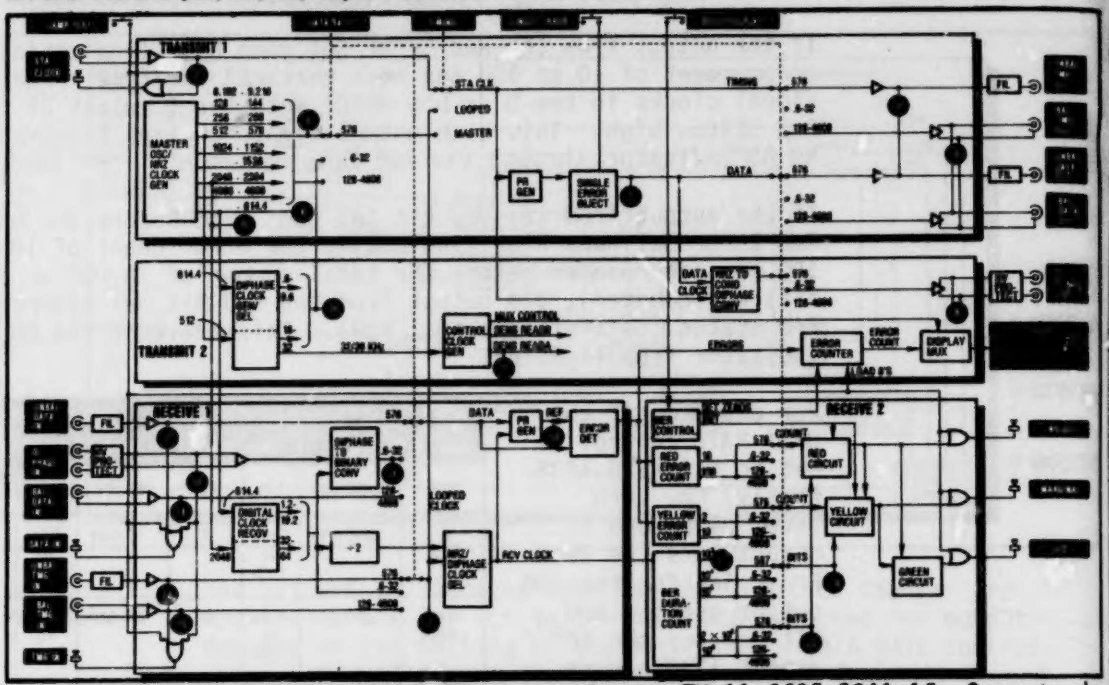
A second output is applied to both the Yellow and Green Lamp Controls. A NO GO indicator inhibits both the MARGINAL and GO indicators.

Yellow Except for the error count of 2 and 10 (instead of 10 or 100) and bit count of 200,000 and 1,000,000 (instead of 10,000 and 100,000), the Yellow circuits operate in the same manner as the Red. The output lights the yellow front panel MARGINAL indicator.

Green Lamp Control A second output from the Yellow Lamp Control is applied to the input of the Green Lamp Control. If the Yellow Lamp Control is active (has lit the yellow MARGINAL indicator) the output to the Green Lamp Control is high, which inhibits the green front panel GO indicator.

If the Yellow Lamp Control is not active, the output to the Green Lamp Control is low, which lights the green front panel GO indicator.

1-20. LOGIC CARDS (A3, A4, A5, A6) INPUT AND FAULT SENSING

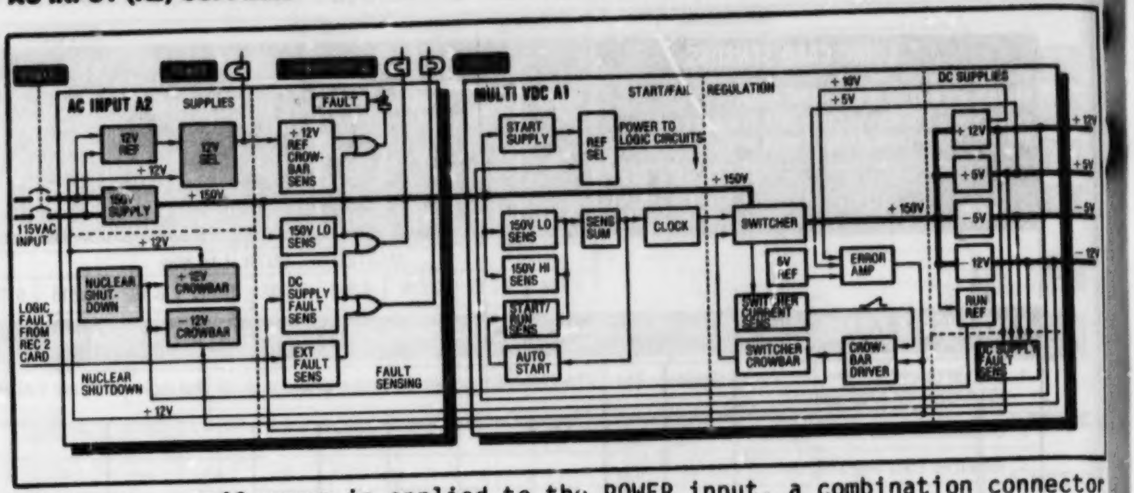


General	For general information refer to TM 11-6625-3041-12, Operator's and Organizational Maintenance Manual. The SG-1139 includes 21 signal sensors. All are enabled regardless of the setting of the TIMING control except sensor 1 Station Clock (enabled in STA CLK mode only), and sensor 17 Looped Clock (enabled in LOOPED Mode only).
Light On With (table head)	Signal - Six sensors are input sensors. When an external input signal is present, they light one (two for diphase inputs) of the front panel indicators (STA CLOCK, DATA IN, and DATA OUT). No sig - Fifteen sensors are fault sensors. When an important internal signal is not present, they light one of the card fault indicators (A3, A4, A5, and A6).
Read Interval (table head)	All sensors except two store activity and are read approximately every 0.25 second (every 2 seconds on Receive 2 card). Whenever the signal they monitor disappears, it can be a 0.25 second or 2 seconds before the fault is indicated. When the signal returns, it can be a 0.25 second or 2 seconds before the indication returns to a no-fault condition. Two sensors are peak detectors and indicate a fault immediately whenever the monitored signal drops below a preset level. When the signal returns to normal, the indicator immediately returns to a no-fault condition.
Data Rate (table head)	Many sensors are enabled only at certain settings of the DATA RATE control such as sensor 3, which is enabled only from 128 to 4608, etc.

-20. LOGIC CARDS (A3, A4, A5, A6) INPUT AND FAULT SENSING (CONT)

LOGIC CARD SENSORS			DATA RATE								
Sensors are enabled in all TIMING modes except sensors 1. Station Clock (STA CLK mode only) and 17. Looped Clock (LOOPED mode only)			UNBAL	DIPHASE			BAL				
NAME	LIGHT ON WITH	READ INTERVAL	576	0.6 1.2 2.4 4.8	9.6	16 32	128	144 288	256 512	576 1,152 1536 2304 4608	1024 2048 4096
			MASTER OSC OUTPUT IN MHz								
			9.216	9.216	9.216	8.192	8.192	9.216	8.192	9.216	8.192
A3 TRANSMIT 1 CARD	A3 fault lamp is inhibited in STA CLK TIMING mode if no signal is present at STA CLOCK input.										
1. Station Clock (STA CLK TIMING mode)	signal	.25s	STA CLK (with no signal, fault indicators on all four logic cards are inhibited.								
2. Unbalanced Data and Tmg Out	no sig	.25s	A3								
3. Balanced Data and Tmg Out	no sig	.25s					A3	A3	A3	A3	A3
4. Master Clock (614.4)	no sig	.25s	A3	A3	A3	A3	A3	A3	A3	A3	A3
5. 512/576 Clock (peak det)	no sig	0s	A3	A3	A3	A3	A3	A3	A3	A3	A3
6. 2048/2304 Clock	no sig	.25s	A3	A3	A3	A3	A3	A3	A3	A3	A3
7. PR Generator	no sig	.25s	A3	A3 Inhibited if no signal present at A4 Diphase Clock sensor	A3	A3	A3	A3	A3	A3	A3
A4 TRANSMIT 2 CARD	A4 fault lamp inhibited if A3 fault lamp is lit or in STA CLK timing mode if no signal is present at STA CLOCK input.										
8. Diphase Out	no sig	.25s		A4	A4	A4					
9. Diphase Clock	no sig	.25s		A4 Inhibits A3 PR Generator sensor	A4	A4					
10. .49/.55Hz Read A (peak det)	no sig	0s	A4	A4	A4	A4	A4	A4	A4	A4	A4
A5 RECEIVE 1 CARD	A5 fault inhibited if A3 or A4 fault lamp is lit or if no signals are present at data and timing inputs, or in STA CLK TIMING mode if no signal is present at STA CLOCK input										
11. Unbalanced Data In	signal	.25s	DATA IN								
12. Unbalanced Tmg In	signal	.25s	TMG IN								
13. Diphase In	signal	.25s		DATA IN, TMG IN							
14. Balanced Data In	signal	.25s					DATA IN				
15. Balanced Tmg In	signal	.25s					TMG IN				
16. Recovered Clock	no sig	.25s		A5	A5	A5	A5				
17. Looped Clock (LOOPED TIMING mode)	no sig	.25s	A5 Inhibits A3 and A4 fault lamps in LOOPED TIMING mode if no signal is present at TMG or DIPHASE inputs.	A5	A5	A5	A5	A5	A5	A5	A5
18. Error Det Reference	no sig	.25s	A5	A5	A5	A5	A5	A5	A5	A5	A5
A6 RECEIVE 2 CARD	A6 fault inhibited if A3, A4, or A5 fault lamp is lit, or if no signals are present at data and timing inputs, or in STA CLK TIMING mode if no signal is present at STA CLOCK input										
19. Yellow End	no sig	2s	A6							A6	A6
20. Red End	no sig	2s	A6		A6	A6		A6	A6	A6	A6
21. BER Duration Counter	no sig	2s	A6	A6	A6	A6	A6	A6	A6	A6	A6

1-21. AC INPUT (A2) SUPPLIES



AC Power AC power is applied to the POWER input, a combination connector and filter FL1 on the rear panel. Both sides are switched by the POWER control circuit breaker CB1 on the front panel. The hot side is applied through a jumper on the Multi VDC card to the 12V and 150V supplies. If the Multi VDC card is removed, the AC Input card is deprived of ac power and will not operate.

12V Ref AC power is applied to the 12V Reference supply where it is stepped down by T1, rectified by CR10, 12, 14, and 16, filtered by C8 and 9, and regulated by VR1.

12V Sel The 12V Reference output is applied to the 12V Sel at the anode of CR25. Two other inputs are applied to the 12V Sel circuit, one at the anode of CR17 (which is not used in the SG-1139) and one at the anode of CR24.

The 12V Reference output is used only during start up. Once the Switcher on the Multi VDC card is operating, the +12V(B) input rises to +12V and backbiases CR25. This prevents the 12V Reference from supplying the 12V(J) line which, instead, is supplied by the normal 12V dc supply (+12V(B)) on the Multi VDC card.

The +12V(J) line is used to power circuits on both the AC Input and Multi VDC cards. It also lights the POWER indicator DS1 on the front panel and supplies power for the ALARM indicators (POWER SUPPLY fault DS2, and FAULT summary DS3) on the front panel.

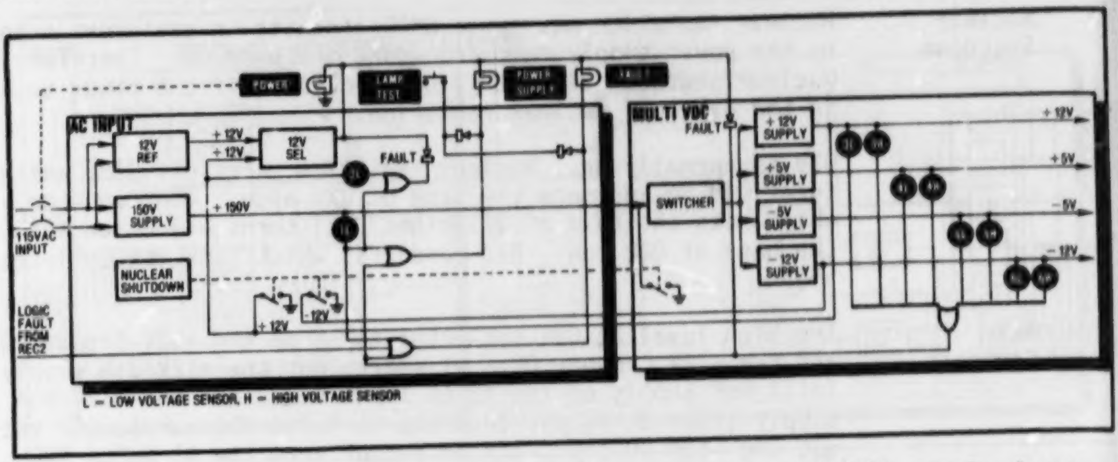
150V Supply AC power is also applied to the 150V supply where it is rectified by CR20 through CR23 and applied through R27 to the Multi VDC card. R27 limits the surge current at turn on.

Once the Switcher on the Multi VDC card is operating, the Soft Start Inh input to Q6 gate goes positive and turns on Q6. With Q6 on, R27 is bypassed and the full current from the 150V Suppl is allowed to pass to the Multi VDC card.

22. AC INPUT (A2) NUCLEAR SHUTDOWN

Nuclear Shutdown	Nuclear radiation may cause CMOS circuits in equipment supplied by the power supply to overconduct and burn up. Therefore, a Nuclear Shutdown circuit is used to turn off the power supply in the event of nuclear radiation.
	Q18 is normally on. Nuclear radiation turns off Q18, which turns Q19 on and sets the base of Q20 high. Q20 turns on, which sets the base of Q21 high. Q21 turns on, which sets the base of Q22 low. Q22 conducts, which sets its collector high.
12V Crowbars	The high level at Q22 collector turns on the +12V Crowbar Q1 and the -12V Crowbar Q2. Q1 shorts out the +12V(J)A supply (+12V Ref supply on the A2 AC Input card) and the +12V(B)A supply (+12V dc output from the A1 Multi VDC card). Q2 shorts out the -12V supply (-12V dc output from the A1 Multi VDC card).
	The high level at Q22 collector is also applied through J1 pin 7 to the input of the Switcher Crowbar on the Multi VDC card. The Switcher Crowbar turns on and shuts down the Switcher, which shuts down the dc supplies.

1-23. AC INPUT (A2) FAULT SENSING

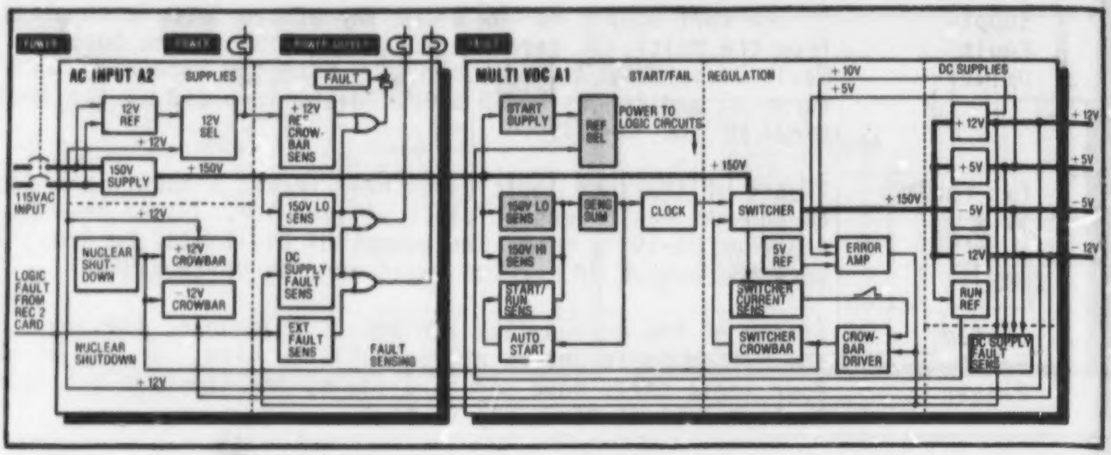


+12V Ref Crowbar Sens	When the +12V Crowbar Q1 turns on, the +12V(J)A supply drops to 0V which sets the negative input of the +12V Ref Crowbar Sens at U1-8 low. This sets the output of U1-14 high, which turns on the AC Input Fault Driver and lights the FAULT lamp DS1 on the AC Input card.
150V Low Sens	If the +150V Supply goes low, the U3 transistor turns off, which turns on Q5 in the 150V Low Sens. With Q5 collector low, the output of U2-15 is high, which turns on the AC Input Fault Driver and lights FAULT lamp DS1 on the AC Input card. The low level at Q5 collector is also applied to U2-9 and 11 whose output at U2-10 and 12 turns on Q24 in the Supply Fault Driver and lights the POWER SUPPLY alarm lamp DS2 on the front panel of the SG-1139.
Board Fault Driver	If either the +12V Crowbar Q1 turns on due to nuclear radiation or the 150V Supply goes low, the Board Fault Driver Q4 turns on FAULT lamp DS1 on the AC Input card.
DC Supply Fault Sens	If any of the four dc supplies from the Multi VDC cards are out of tolerance, the input to the DC Supply Fault Sens at U6-1 and 2 is low. With the input low, the output at U6-3 is high and at U6-4 is low. With U6-4 low, the output of U8-2 and 4 is high, which turns on Q24 in the Supply Fault Driver. With Q24 on, POWER SUPPLY alarm lamp DS2 lights on the front panel of the SG-1139. The output of U8-2 and 4 is also applied to the input of the System Fault Driver and lights FAULT alarm lamp DS3 on the front panel of the SG-1139.

1-23. AC INPUT (A2) FAULT SENSING (CONT)

Supply Fault Driver	If the 150V Supply is low or if any of the four dc supplies from the Multi VDC card are low, the input to the Supply Fault Driver at Q24 base is high. With its base high, Q24 turns on and lights POWER SUPPLY alarm lamp DS2 on the front panel of the SG-1139.
Ext Fault Sens	If any of the four logic cards have sensed a fault, the input to the Ext Fault Sens at U1-11 will be low. Since the negative input at U1-10 is high, the output of U1-13 will be low. This sets the output of the Ext Fault Sens at U8-15 high.
System Fault Driver	If any of the dc supplies are out of tolerance, the input to the System Fault Driver at U6-9 will be high. If any of the four logic cards have sensed a fault, the input to the System Fault Driver at U6-8 will be high. If either input is high the output at U6-10 is low, which sets the output of U8-12 high and the output of U8-10 low. With U8-10 low, Q3 turns off and deenergizes K1. This provides FAULT alarm lamp DS3 on the front panel of the SG-1139 with a return through K1-B3 and B2 and lights DS3.

1-24. MULTI VDC (A1) START



Start Supply

① At turn on, the 150V Supply output at J2-21 begins to rise towards +150V. When it reaches 15 to 25V, VR1 in the Start Supply conducts and produces a +10V Ref output at its cathode.

② The +10V Ref voltage turns on Q1, which produces a +9V output at its emitter. Because there is yet no +12V Run Ref input at CR4 anode, the +9V Start Ref voltage is used as the Ref Power voltage and powers the Sens, Sens Sum, and Clock circuits.

150V Hi Sens

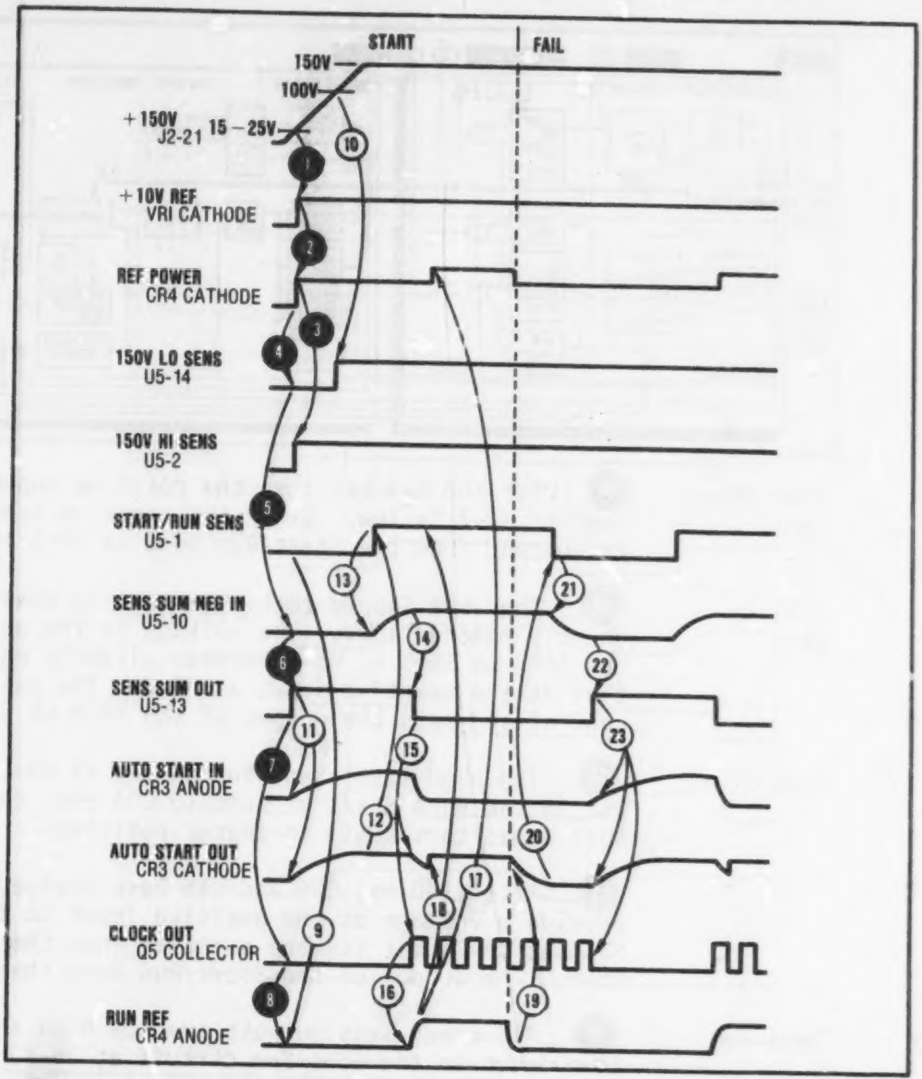
③ The negative input to the 150V Hi Sens at U5-4 is derived from voltage divider R29-R63-R65 and is 1/20 the voltage applied at the top. The applied voltage is from the 150V Supply so that the negative input at U5-4 would normally rest at 1/20 x 150V = 7.5V. But the 150V Supply at this time is well under 150V, so the negative input at U5-4 is only slightly over +1V.

The voltage at the positive input at U5-5 is derived from voltage director R71-R72 and is one-half the voltage applied at the top. The applied voltage is the Ref Power which, at this time, is the +10V Ref voltage so that the voltage at U5-5 is 1/2 x 10V = 5V. Therefore, the voltage at the positive input is more positive than that at the negative input. The positive input takes control and sets the output of the 150V Hi Sens at U5-2 high.

150V Lo Sens

④ The negative input to the 150V Lo Sens at U5-8 is +5V, which is more positive than the positive input at U5-9. The negative input takes control and sets the output of the 150V Lo Sens at U5-14 low.

1-24. **MULTI VDC (A1) START** (CONT)



Sens Sum

❺ The outputs from all three Sens circuits are connected together. A low output from any Sens circuit causes a low level at the negative input of the Sens Sum circuit at U5-10.

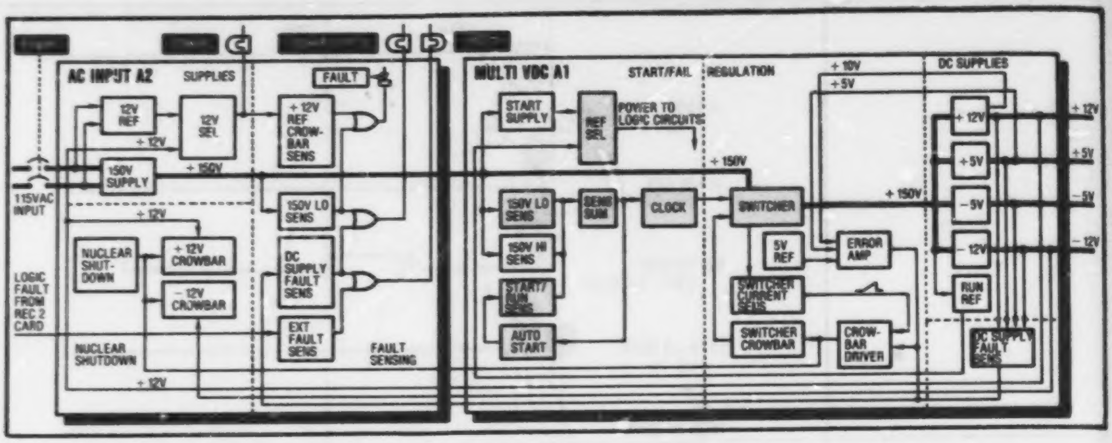
❻ The positive input to the Sens Sum circuit at U5-11 is +5V, which is more positive than the negative input at U5-10. The positive input takes control and sets the output of the Sens Sum circuit at U5-13 high.

❼ The high-level Sens Sum output inhibits the Clock output. The Clock output drives the Switcher. Thus, with the Clock inhibited, the Switcher is off.

Ref Sel

❽ With the Switcher off no dc outputs are available, including that from the Run Ref whose output is low.

1-24. MULTI VDC (A1) START (CONT)



Start/Run Sens

⑨ With the Run Ref low, the positive input to the Start/Run Sens at U5-7 is low. Since the negative input at U5-6 is high, the output from the Start/Run Sens at U5-1 is low.

150V Lo Sens

⑩ The 150V Supply continues to rise towards 150V and shortly reaches 100V. The voltage to the positive input of the 150V Lo Sens at U5-9 becomes slightly more positive than that at the negative input at U5-8. The positive input takes control and sets the output of the 150V Lo Sens at U5-14 high.

Auto Start

⑪ The high-level Sens Sum output at U5-13 is applied through R69 in the Auto Start circuit to C64 and, through CR3, to C66. Both capacitors begin to charge positive.

⑫ After 100 ms, C64 and C66 have charged sufficiently to provide a voltage at the positive input to the Start/Run Sens at U5-7 that is more positive than the negative input at U5-6. The output of the Start/Run Sens then goes high.

Sens Sum

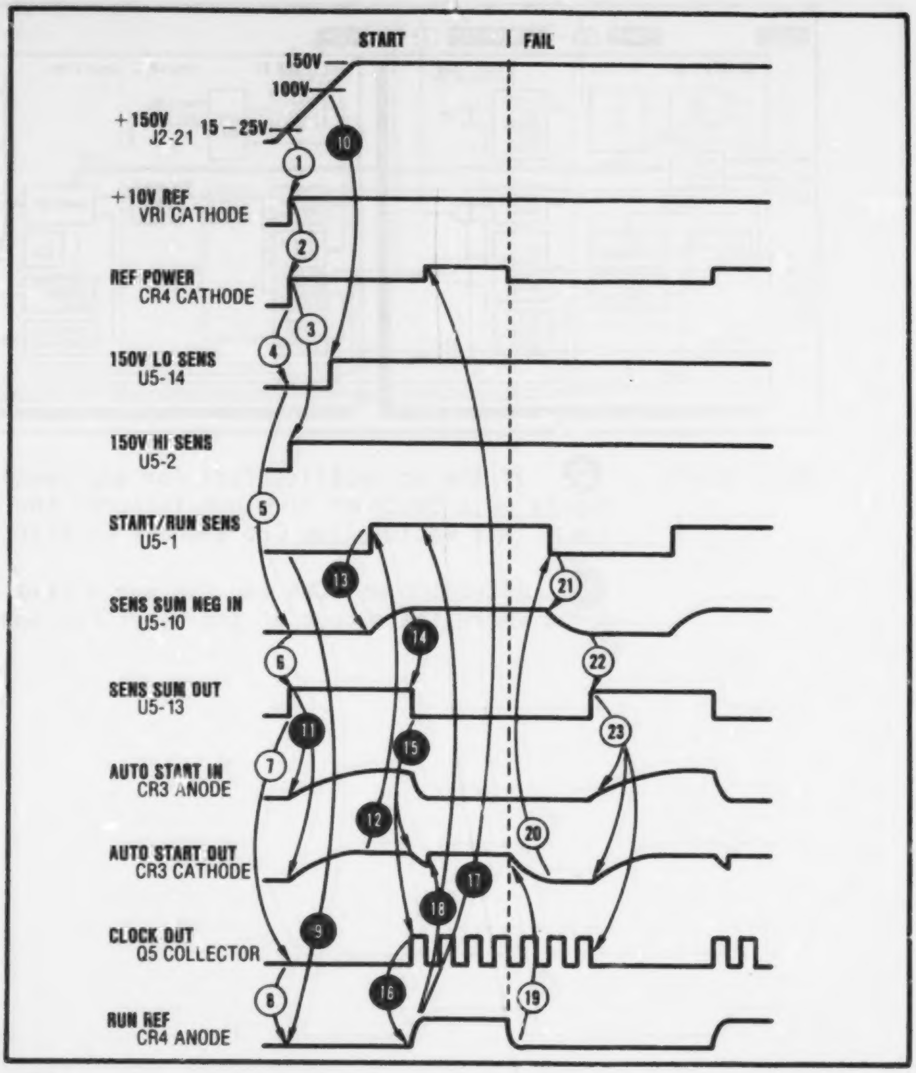
⑬ All three Sens outputs are now high and C62 at the negative input to the Sens Sum circuit at U5-10 begins to charge through R51.

⑭ C62 eventually changes sufficiently to cause the negative input to the Sens Sum circuit at U5-10 to be more positive than the +5V at the positive input. This sets the output of the Sens Sum circuit at U5-13 low.

Clock

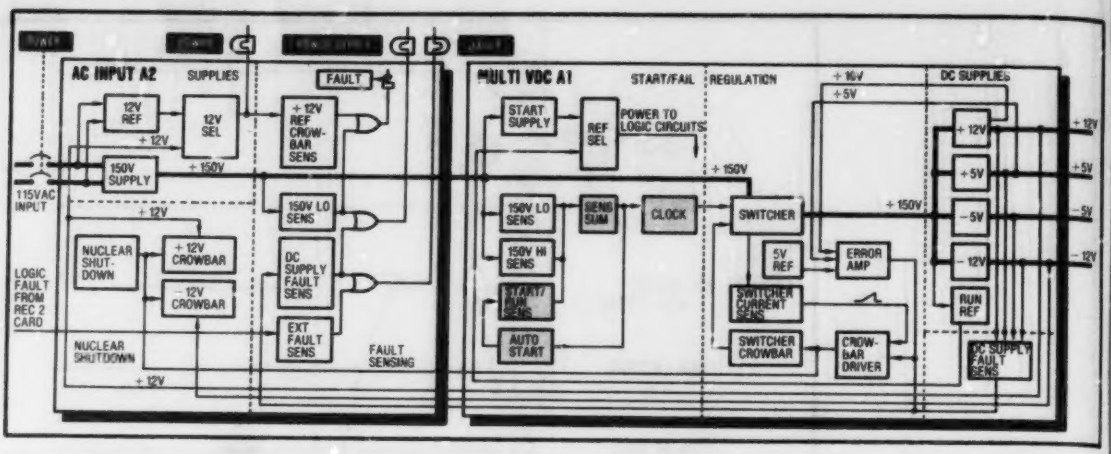
⑮ When the Sens Sum output at U5-13 goes low, C64 begins to discharge through R68 and CR1 and C66 begins to discharge throug R67. The low-level Sens Sum output also enables the Clock, whic produces a 22 kHz (nominal) output that drives the Switcher.

1-24. MULTI VDC (A1) START (CONT)



Switcher	⓰ With the Switcher running dc outputs are available, including that from the Run Ref whose output is +12V.
Ref Sel	⓱ The +12V Run Ref is applied through CR4 in the Ref Sel circuit and backbiases Q1, which turns off. The Ref Power voltage thus becomes the +12V Run Ref and is used to maintain power to the Sens, Sens Sum, and Clock circuits.
Start/Run Sens	⓲ The +12V Run Ref voltage is also applied to the top of voltage divider R66-R64. The voltage at the junction of R66-R64 is 1/2 x 12V = 6V and is applied through CR37 to the positive input of the Start/Run Sens at U5-7. This keeps the output of the Start/Run Sens at U5-1 high, which keeps the Clock and the Switcher running.

1-25. MULTI VDC (A1) FAIL

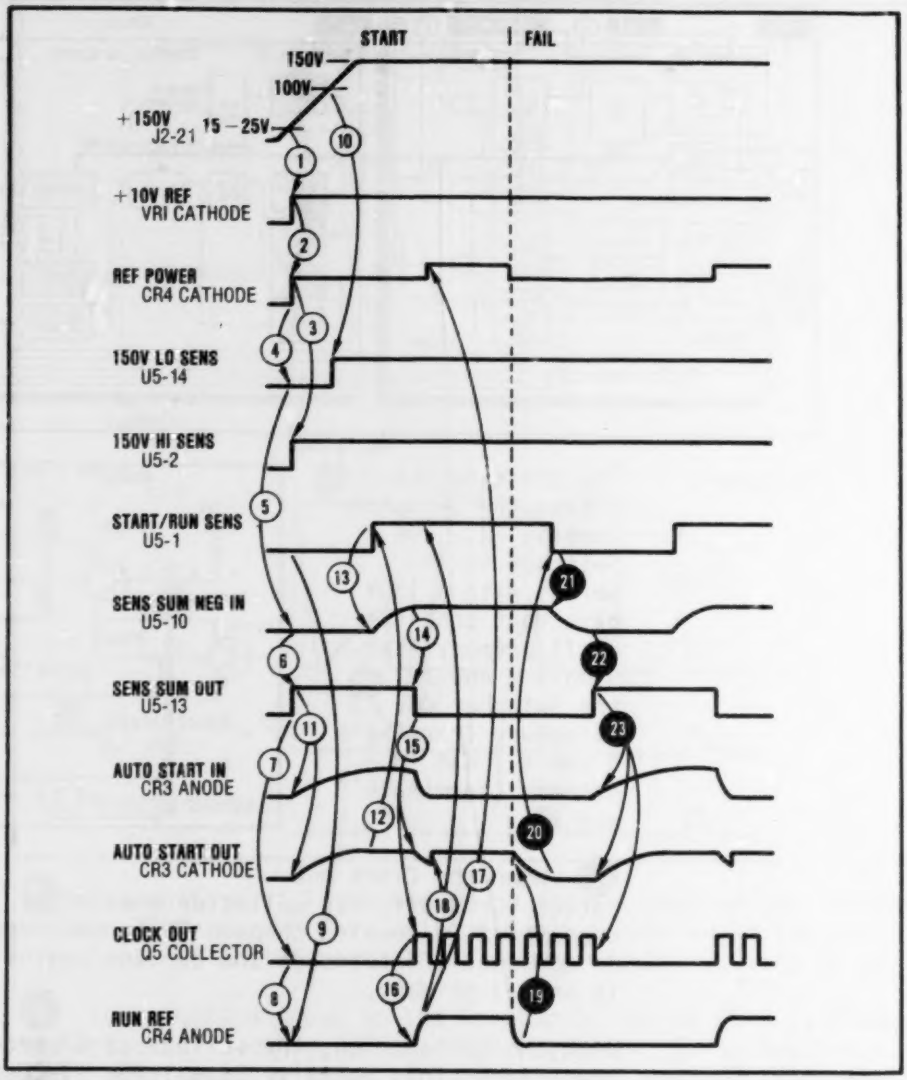


Auto Start

⑲ If the dc supplies fail for any reason (e.g., a shorted supply or a Switcher or Clock failure) the Run Ref would go low. This would allow C66 and C64 to start discharging.

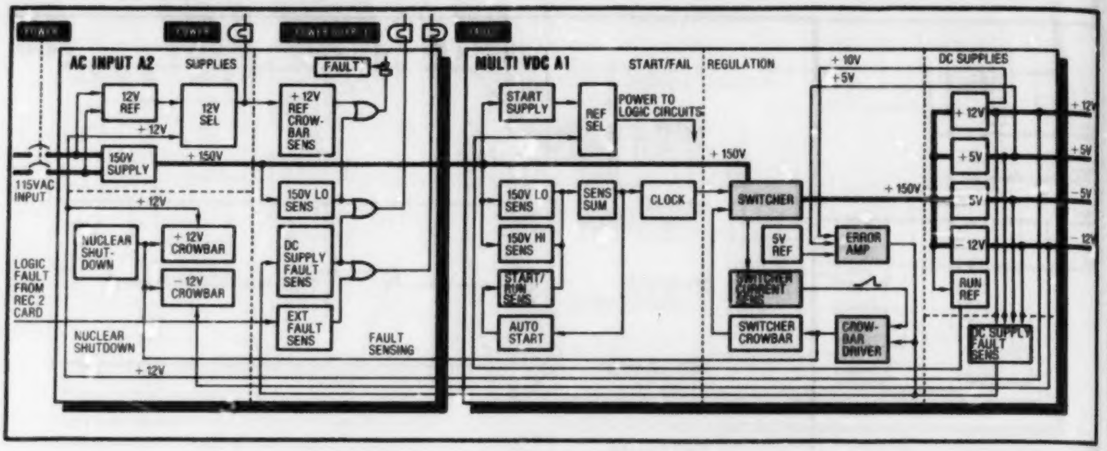
⑳ After 100 ms, C66 and C64 would have discharged to the point where the output of the Start/Run Sens at U5-1 goes low.

1-25. **MULTI VDC (A1) FAIL** (CONT)

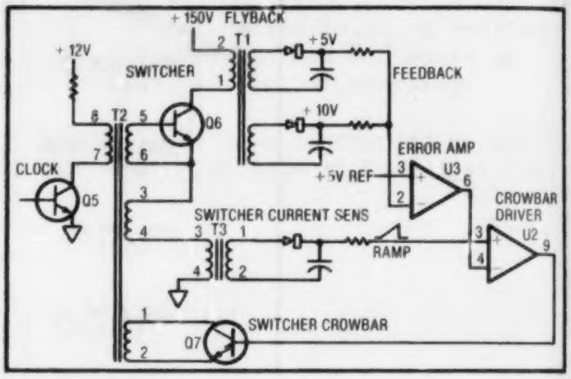


Start/Run Sens	㉑ The low-level output of the Start/ Run Sens begins to discharge C62 through R51 at the negative input of the Sens Sum circuit.
Sens Sum	㉒ C62 eventually discharges sufficiently to cause the Sens Sum output at U5-13 to go high.
Clock	㉓ The high-level Sens Sum output stops the Clock (if not already stopped) and allows C64 and C66 in the Auto Start circuit to begin charging, thus beginning a new start cycle.

1-26. MULTI VDC (A1) REGULATION



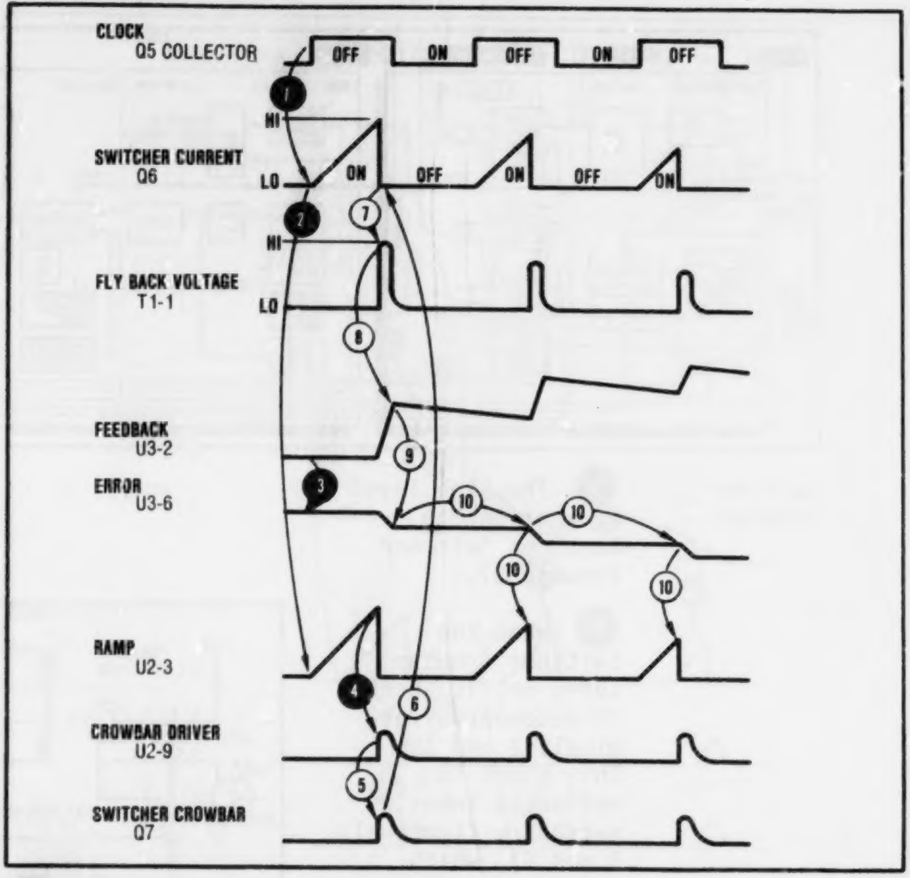
Switcher The Clock output drives the Switcher through T2. The Switcher is in series with a 150V path that consists of T1 primary (terminals 2 and 1), the Switcher Q6, T2 secondary (terminals 3 and 4), and T3 primary (terminals 3 and 4).



① When the Clock output Q5 turns off, its collector goes high. This positive transition is coupled through T2 to the input of the Switcher at Q6 base. Q6 turns on and current begins to increase through it and T3 primary.

With the Switcher on, the voltage at T2 secondary terminal 3 goes high. This positive transition is coupled back to T2 secondary terminal 5 at the base of Switcher Q6, which reinforces the positive voltage from the Clock output in a positive feedback loop similar to a multivibrator.

1-26. MULTI VDC (A1) REGULATION (CONT)



Switcher Current Sens

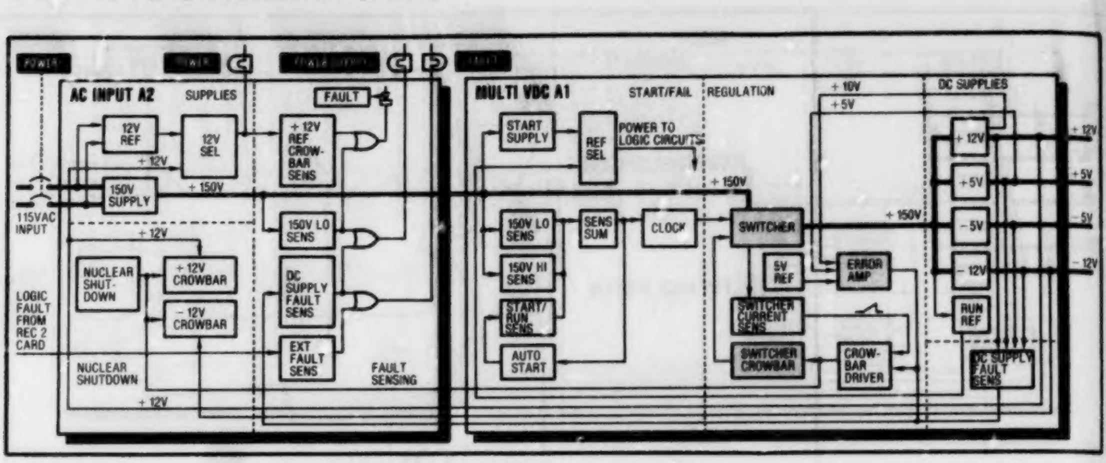
❷ The voltage at T3 secondary is proportional to the current through T3 primary. This voltage ramp is applied to the positive input of a differential amplifier (Crowbar Driver) at U2-3.

Crowbar Driver, Error Amp

❸ The negative input to the Crowbar Driver at U2-4 is from the output of another differential amplifier (Error Amp) at U3-6. The positive input at U3-3 is a constant +5V reference voltage. The negative input at U3-2 is a feedback voltage derived from the +5V and +10V dc supplies. At turn on the dc supplies are at zero so that the output of the Error Amp at U3-6 is high (about +11.8V).

❹ As the ramp voltage rises, it eventually becomes more positive than the error voltage at U2-4 from the Error Amp output. This sets the Crowbar Driver output at U2-9 high.

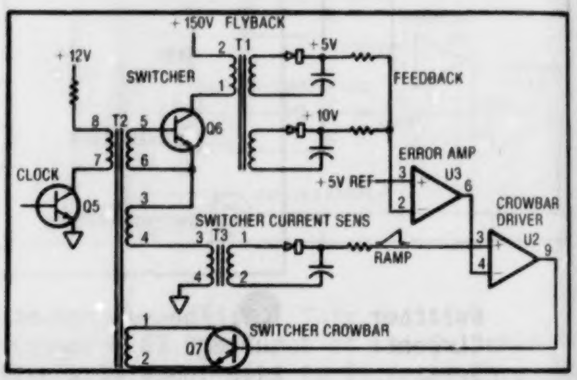
1-26. MULTI VDC (A1) REGULATION (CONT)



Switcher Crowbar

⑤ The high level Crowbar output turns on Switcher Crowbar Q7.

⑥ When the Switcher Crowbar turns on, it shorts T2 secondary (terminals 2 and 1). This short is reflected into T2 secondary (terminals 5 and 6), which shorts Q6 base to emitter and turns off the Switcher.



The Clock cannot turn off the Switcher because it lacks sufficient power to control the Switcher current, which can be several amperes.

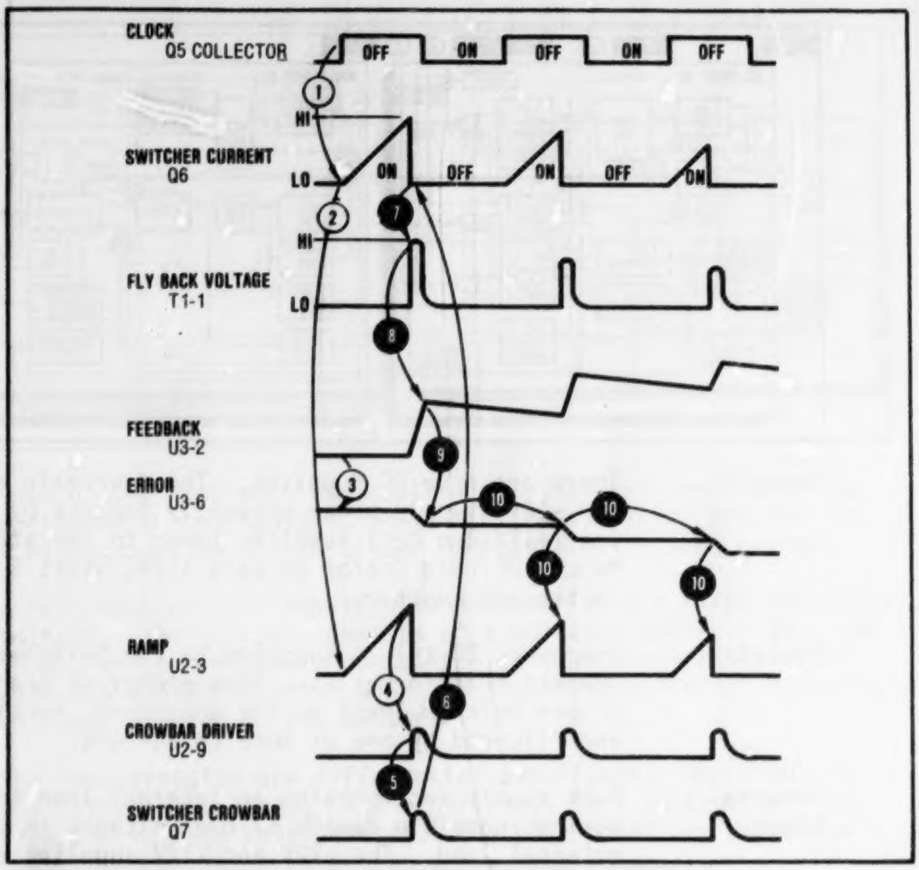
The Switcher Crowbar remains on only momentarily. Once it shorts the secondary it no longer has an anode supply sufficient to keep it conducting.

Switcher

⑦ When the Switcher turns off, the rapid decrease in current induces a high voltage in the secondaries of flyback transformer T1.

⑧ These secondaries supply power for all four dc supplies, including the +5V and +10V supplies used for the feedback voltage to the negative input to the Error Amp.

1-26. MULTI VDC (A1) REGULATION (CONT)



Error Amp ⑨ As the dc supplies (including the feedback voltage) charge up, the output of the Error Amp at U3-6 decreases.

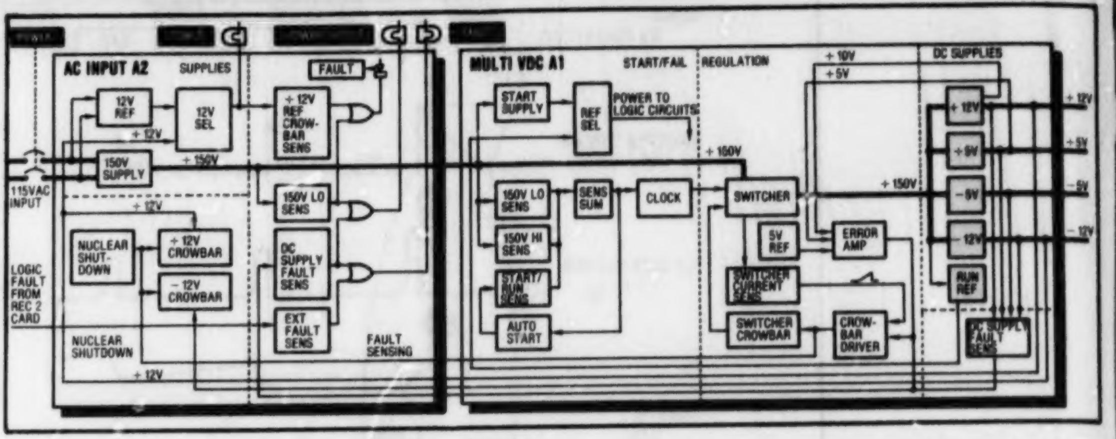
⑩ As the Error Amp output decreases on successive clock cycles, the ramp voltage at U2-3 (required to turn on the Switcher Crowbar) decreases.

Switcher With less and less ramp voltage required to turn off the Switcher, the Switcher turns off earlier and earlier (i.e, the Switcher turns off with less and less current flowing through it). This results in less and less energy being transferred to the flyback secondaries.

Thus, as the dc supplies reach their proper value, they receive less and less energy from the Switcher. In fact, they receive only enough energy to keep them within ±5 percent of their proper value, as determined by the +5V and +10V supplies used to provide the feedback voltage.

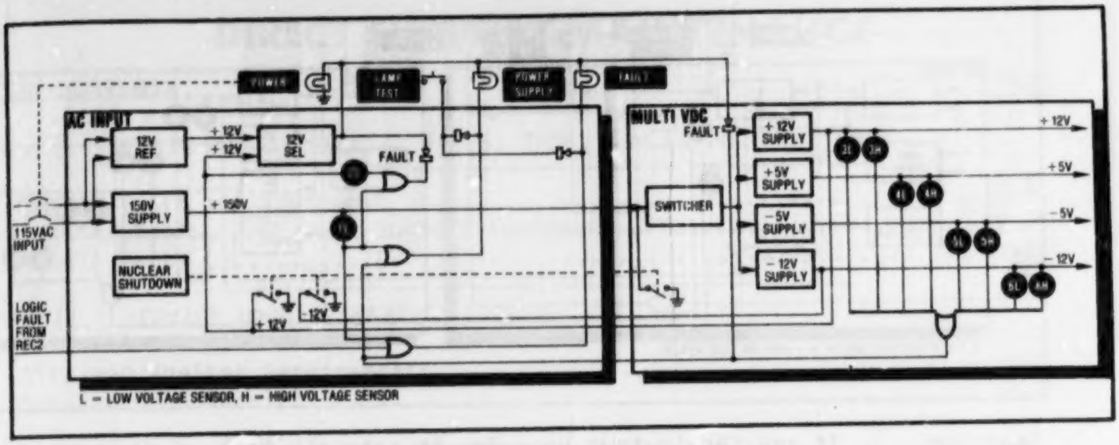
Because of the loads on the supplies, they are constantly discharging, which requires the Switcher to supply some energy on every Clock cycle.

1-27. MULTI VDC (A1) DC SUPPLIES



General	There are five DC Supplies. The four main ones (+12, +5, -5, and -12V) supply power primarily for use by external circuitry. One (+12V Run Ref) supplies power to the start circuitry on the Multi VDC card (refer to para 1-24, Start Supply). All operate in the same manner.
Operation	Energy at 20 kHz is supplied by the Switcher to the primary of flyback transformer T1. This energy is transformed to the proper voltage level at the secondary, rectified by a diode, and filtered by one or more capacitors.
Internal Loads	Each supply incorporates an internal load to protect the supply against possible damage by overvoltages in the absence of an external load. The +12V and -12V supplies use a 511-ohm resistor at the output. The +5V supply uses a 56 ohm resistor at the output. The -5V supply uses a 20.5-kilohm resistor located in the fault sensing reference circuit. The +12V Run Ref uses two 511-ohm resistors located in the Ref Sel circuit.
Dual Voltages	The secondary windings for the +12V and -12V DC Supplies include a tap so that these supplies can be used to supply either 12 or 10V.

1-28. MULTI VDC (A1) FAULT SENSING



L — LOW VOLTAGE SENSOR, H — HIGH VOLTAGE SENSOR

General Each of the four main DC Supplies (+12, +5, -5, and -12V) is monitored by two sensors, one for a low condition and one for a high condition. Each sensor operates in the same manner.

Reference A Reference circuit provides each sensor with a fixed reference voltage. The circuit consists of a voltage regulator (R91 and VR12), which provides a constant 5.1V; and a voltage divider (R34-R35-R36-R37), which provides the three different reference voltages applied to the sensor.

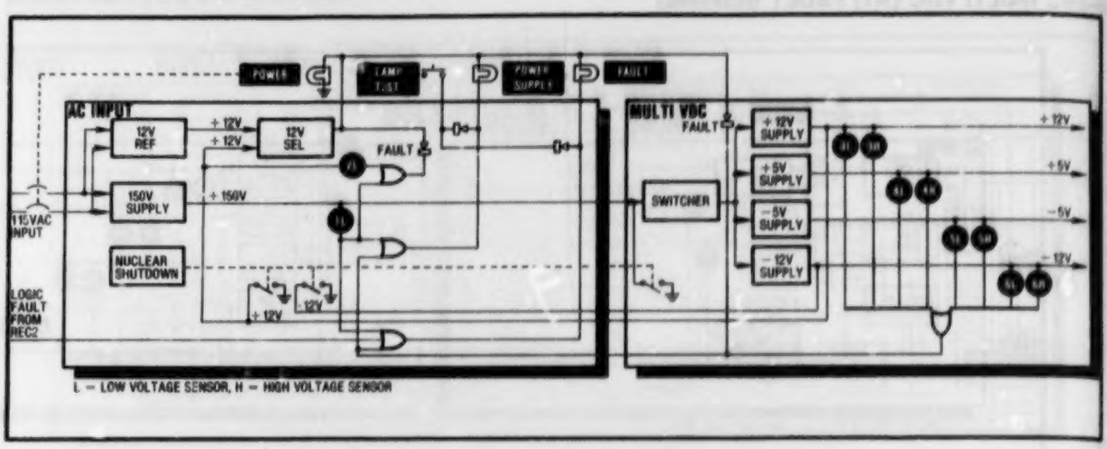
Sensors The Sens circuits are differential amplifiers. One input is the reference voltage. The other input is a voltage derived from the voltage being sensed. The thresholds are as follows:

Supply	Low Threshold	High Threshold
+12V	+7.6 to +9.0V*	+11.2 to +12.6V*
+5V	+4.1 to +4.6V	+5.7 to +6.9V
-5V	-3.1 to -4.6V	-5.9 to -6.9V
-12V	-8.1 to -9.8V	-13.1 to -14.8V

*Actual voltage sensed is +10V for which low threshold is +7.6 to +9.0V and high threshold +11.2 to +12.6V.

Normally the output from each sensor is high. An out-of-tolerance voltage input causes the sensor output to go low.

1-28. MULTI VDC (A1) FAULT SENSING (CONT)



Sens Sum

If any Sens output goes low it sets the base of Q4 low. Q4 conducts and sets the base of Q3 high, which conducts and lights board fault lamp DS1. It also applies a high level to the DC Supply Fault Sens circuit on the AC Input card, which lights both the POWER SUPPLY and FAULT front panel lamps.

If any Hi Sens output goes low it not only lights the fault lamps, but also applies low level to the Crowbar Driver negative input at U2-4. This sets the output of the Crowbar Driver high, which turns on the Switcher Crowbar and prevents the Switcher from operating.

Chapter 2

DIRECT SUPPORT MAINTENANCE

CHAPTER CONTENTS

Page

Section I. REPAIR PARTS, SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

2-1. Common Tools and Equipment 2-2
2-2. Special Tools, TMDE, and Support Equipment 2-2
2-3. Repair Parts 2-2

Section II. SERVICE UPON RECEIPT

2-4. Site and Shelter Requirements 2-2
2-5. Service Upon Receipt 2-2

Section III. **EQUIPMENT CHECK PROCEDURES**

2-6. **SG-1139 Check Procedure** **2-3**
2-7. **Power Cable Check Procedure** **2-27**
2-8. **Interface Box Check Procedure** **2-28**

Section IV. PREVENTIVE MAINTENANCE CHECKS AND SERVICES

2-9. Monthly Preventive Maintenance 2-29

Section V. TROUBLESHOOTING

2-10. Troubleshooting 2-29

Section VI. **MAINTENANCE PROCEDURES**

2-11. **Reference Maintenance Procedures** **2-29**
2-12. **Knob Replacement** **2-30**
2-13. **Control Filter Replacement** **2-31**
2-14. **LED Indicator Replacement** **2-32**
2-15. **Pushbutton Replacement** **2-33**
2-16. **Power Cable Repair** **2-34**
2-17. **Interface Box Repair** **2-40**

Section VII. PREPARATION FOR STORAGE OR SHIPMENT

2-18. Short-Term Storage **2-44**

Section I.

REPAIR PARTS, SPECIAL TOOLS LIST (RPSTL) TEST, MEASUREMENT, AND DIAGNOSTIC EQUIPMENT (TMDE) SUPPORT EQUIPMENT

2-1 . COMMON TOOLS AND EQUIPMENT

There are no common tools and test equipment for Digital Data Generator SG-1139/G.

2-2 . SPECIAL TOOLS, TMDE, AND SUPPORT EQUIPMENT

For Repair Parts and Special Tools List (RPSTL), refer to TM 11-6625-3041-30 Direct Support Maintenance RPSTL.

Maintenance tools and equipment as authorized by the Maintenance Allocation Chart (refer to TM 11-6625-3041-12 Operator's and Organizational Maintenance Manual, Appendix B MAC) for general support maintenance are as follows:

1 ea TK-101/G Tool Kit, Electronic Equipment
1 ea AN/PSM-45 Digital Multimeter
1 ea PACE PRC-350C Bench Top Repair Facility

2-3 . REPAIR PARTS

Repair parts are listed and illustrated in TM 11-6625-3041-30P, Direct Supp Maintenance Repair Parts and Special Tools List.

Section II .

SERVICE UPON RECEIPT

2-4 . SITE AND SHELTER REQUIREMENTS

For site and shelter requirements, refer to TM 11-6625-3041-12, Operator's and Organizational Maintenance Manual.

2-5 . SERVICE UPON RECEIPT

For service upon receipt, refer to TM 11-6625-3041-12, Operator's and Organizational Maintenance Manual.

Section III

EQUIPMENT CHECK PROCEDURES

2-6. SG-1139 CHECK PROCEDURE

Purpose

To localize to a major assembly any problem with the operation of the SG-1139.

Major Assemblies

Major Assembly	Associated Check Step
Case Assembly	1 2 3 . . . . . . 10 . . . . . .
AC Input card	1 2 . . . .
Multi VDC card ...	. 2 3 4 . . . .
Transmit 1 card ..	. . 3 4 5 . . . . . . 12 13 . . .
Transmit 2 card ..	. . . 4 . 6 . . . . 11 12 13 . . .
Receive 1 card ...	. . . . . . 7 8 9 10 . 12 . . . .
Receive 2 card ...	. . . . 13 14 15 16
Control Filter ...	. . . 4 5 6 7 8 9 10 11 12 13 . . .

Procedure

Each step in the procedure serves as a foundation for the next. Therefore, each step must be performed in the order given. If they are not, the information given under "This step checks the following:" and the "possible cause" information is invalid.

Fault Lamps

Trouble analysis is aided by fault lamps on the front panel (FAULT and POWER SUPPLY) and on each circuit card. If these are not working, however, this procedure can still be used but it will take longer to perform.

Indications

Any observed front-panel indications that are not specifically called out in the procedure can be ignored.

Indicators

Indicators are illustrated as follows:

◎ White (blank) .. Not lit or can be ignored

◐ Half black ..... Blinking

● Black .... Lit

Equipment Required

a. TK-101/G Tool Kit, Electronic Equipment, for 1/4-in. socket wrench or flat-tip screwdriver.

b. Cables terminated in triaxial connectors.

c. BNC cables, 2 ea, supplied as accessories.

d. BNC adapters, 2 ea, supplied as accessories.

2-6. SG-1139 CHECK PROCEDURE (CONT)

Step 1 Power Input

- Disconnect all cables from front panel connectors.
- Connect SG-1139 to a source of 115 Vac power and set POWER to ON:

Green POWER indicator must light. If it does, proceed to step 2.

This step checks the following:

External	115 Vac power outlet
Accessory	Power cable
AC Input card	12V Ref circuit
Case Assembly	POWER input connector POWER circuit breaker POWER indicator

If POWER indicator does not light:

Press LAMP TEST pushbutton. If any other indicator lights, possible cause is POWER indicator lamp. Replace (refer to TM 11-6625-3041-12), and repeat step 1.

If no indicator lights when LAMP TEST pushbutton is pressed, possible cause is 115 Vac power outlet. Check outlet. If power is missing, connect SG-1139 to an outlet in which power is present and repeat step 1.

If outlet is functional, possible cause is power cable. Replace or repair (refer to para 2-15), and repeat step 1.

If replacement power cable does not provide proper indication, possible cause is AC Input card A2. Replace (refer to TM 11-6625-3041-12), and repeat step 1.

If replacement AC Input card does not provide proper indication, possible cause is POWER input connector or POWER circuit breaker. Evacuate equipment to depot for repair.

2-6. **SG-1139 CHECK PROCEDURE** (CONT)

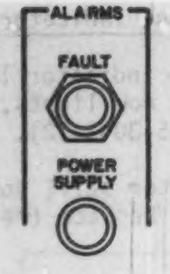
Step 2 Alarm Indicators

- Set controls as follows:

  POWER ... ON

  TIMING .. STA CLK

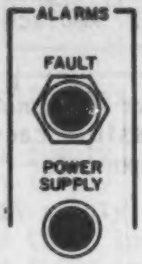
  Red FAULT and POWER SUPPLY alarm indicators must not be lit



- Press and hold LAMP TEST pushbutton:

  Red FAULT and POWER SUPPLY alarm indicators must light.

  If both parts of this step pass, release LAMP TEST pushbutton and proceed to step 3.



This step checks the following:

AC Input card ... 150V supply
Multi VDC card .. All
Case Assembly ... LAMP TEST pushbutton
Alarm indicators

If both indicators are lit before LAMP TEST is pressed:

Remove POWER SUPPLY access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card (if both cards contain a lit indicator, or if no card contains a lit indicator, replace AC Input card A2), and repeat step 2.

If one indicator is lit before LAMP TEST is pressed:

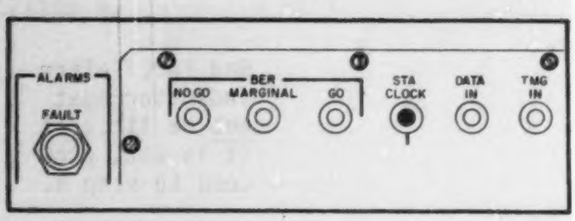
Replace AC Input Card A2 (refer to TM 11-6625-3041-12), and repeat step 2.

2-6 . SG-1139 CHECK PROCEDURE (CONT)

Step	
2 cont	If only one indicator lights when LAMP TEST is pressed: Swap that indicator lamp with the POWER indicator lamp. If indicator now lights, cause is lamp. Replace (refer to TM 11-6625-3041-12), and repeat step 2. If indicator still does not light, possible cause is AC Input card A2. Replace (refer to TM 11-6625-3041-12), and repeat step 2. If neither indicator lights when LAMP TEST is pressed: Swap one indicator lamp with the POWER indicator lamp. If indicator now lights, cause is both FAULT and POWER SUPPLY indicators. Replace (refer to TM 11-6625-3041-12), and repeat step 2. If indicator does not light, nor do any other front panel indicators, possible cause is LAMP TEST pushbutton. Evacuate to direct support for repair.

2-6. **SG-1139 CHECK PROCEDURE** (CONT)

Step	Station	
3	Clock Indicator	• Set controls as follows: POWER ... ON TIMING .. STA CLK Press and hold LAMP TEST pushbutton: Green STA CLOCK indicator must light. If it does, release LAMP TEST pushbutton and proceed to step 5.



This step checks the following:

Multi VDC card	+5V supply -5V supply -12V supply
Transmit 1 card ...	STA CLOCK lamp driver
Case Assembly	STA CLOCK indicator lamp

If STA CLOCK indicator is lit before LAMP TEST is pressed:

Possible cause is Multi VDC card A1 (-12V supply defective). Replace (refer to TM 11-6625-3041-12), and repeat step 3.

IF STA CLOCK indicator does not light:

Possible cause is Transmit 1 card A3. Replace (refer to TM 11-6625-3041-12), and repeat step 4.

If replacement Multi VDC card A1 does not provide proper indication, possible cause is STA CLOCK indicator lamp. Replace (refer to para 2-13), and repeat step 3.

2-6. SG-1139 CHECK PROCEDURE (CONT)

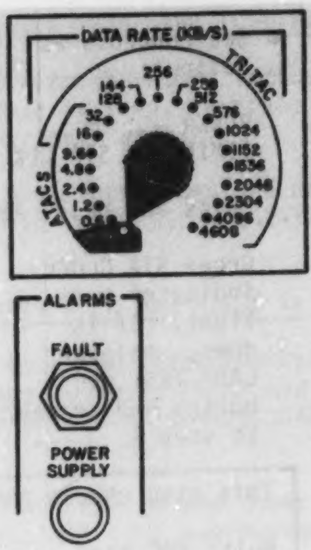
Step 4 Unbalanced NRZ Out

- Set controls as follows:

POWER ...... ON

TIMING ..... MASTER
DATA RATE .. 576 ATACS

Red FAULT alarm indicator must not be lit. If it is not, proceed to step 5.



This step checks the following:

Multi VDC card	+12V supply
Transmit 1 card ...	Master timing select 576 family data rate decode and select Master Osc at 9.216 MHz NRZ Clock Gen at 576 kHz PR Gen Single Error Inject UNBALANCED TMG OUT circuits UNBALANCED DATA OUT circuits
Transmit 2 card ...	Control Clock Gen
Control Filter	TIMING control MASTER setting DATA RATE control 576 family setting

If FAULT alarm indicator is lit:

Remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 4.

If replacement card does not provide proper indication, possible cause is Control Filter A8. Replace (refer to para 2-13), and repeat step 4.

If no logic card contains a lit fault indicator, remove POWER SUPPLY access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 4.

6. SG-1139 CHECK PROCEDURE (CONT)

tep

ont

If no card contains a lit fault indicator, possible cause is (in order of probability): Transmit 1 card A3, Transmit 2 card A4, and Multi VDC card A1. Replace, one at a time (refer to TM 11-6625-3041-12), and repeat step 4.

If none of these replacement cards provide the proper indication, possible cause is Control Filter A8. Replace (refer to para 2-13), and repeat step 4.

2-6. SG-1139 CHECK PROCEDURE (CONT)

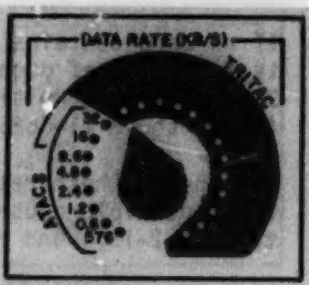
Step 5 Balanced NRZ Out

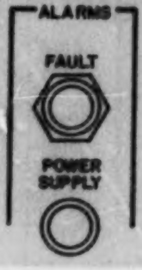
- Set controls as follows:

POWER ... ON
TIMING .. MASTER

Set DATA RATE to 128 through 4096;

At each setting, FAULT indicator must not be lit. If it is not, proceed to step 6.





This step checks the following:	
Transmit 1 card ...	128-4068 family data rate decode and select Master Osc at 8.192 MHz NRZ Clock Gen at 128 through 4608 kHz BALANCED TMG OUT circuits BALANCED DATA OUT circuits
Control Filter	DATA RATE control 128-4608 family settings

If FAULT indicator is lit at any setting:

Remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 5.

If no card contains a lit fault indicator, possible cause is Transmit 1 card A3. Replace (refer to TM 11-6625-3041-12), and repeat step 5.

If replacement card does not provide proper indication, possible cause is Control Filter A8. Replace (refer to para 2-13), and repeat step 5.

2-6. SG-1139 CHECK PROCEDURE (CONT)

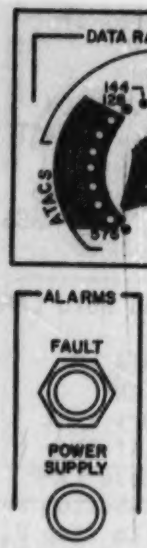
Step 6 Diphase Out

- Set controls as follows:

POWER .... ON
TIMING ... MASTER

Set DATA RATE to 0.6 through 32:

At each setting, FAULT indicator must not be lit. If it is not, proceed to step 7.



This step checks the following:	
Transmit 2 card ...	Diphase Clock Gen/Sel NRZ to Cond Diphase Conv DIPHASE OUT circuits
Control Filter	DATA RATE control .6-32 family settings

If FAULT indicator lights at any setting:

Remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 6.

If no card contains a lit fault indicator, possible cause is Transmit 2 card A4. Replace (refer to TM 11-6625-3041-12), and repeat step 6.

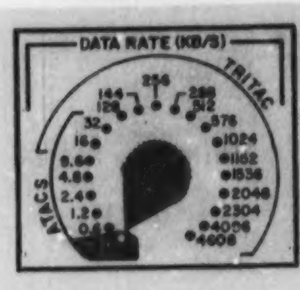
If replacement card does not provide proper indication, possible cause is Control Filter A8. Replace (refer to para 2-13), and repeat step 6.

2-6. SG-1139 CHECK PROCEDURE (CONT)

Step 7 Input Indicators

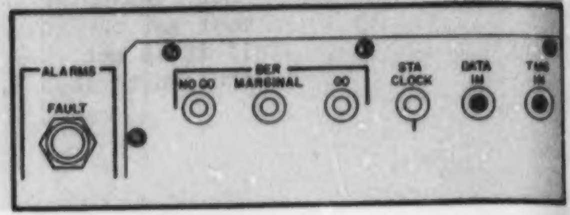
- Set control as follows:

POWER ...... ON
TIMING ..... MASTER
DATA RATE .. 576 ATACS



Press and hold LAMP TEST pushbutton:

Green DATA IN and TMG IN indicators must light. If they do, release LAMP TEST pushbutton and proceed to step 8.



This step checks the following:

Receive 1 card ...	DATA IN lamp driver TMG IN lamp driver
Control Filter ...	DATA IN indicator lamp TMG IN indicator lamp

If DATA IN or TMG IN indicator does not light:

Remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 7.

If no card contains a lit fault indicator, possible cause is Receive 1 card A5. Replace (refer to TM 11-6625-3041-12), and repeat step 7.

If replacement card does not provide proper indication, possible cause is Control Filter A8. Replace (refer to para 2-13), and repeat step 7.

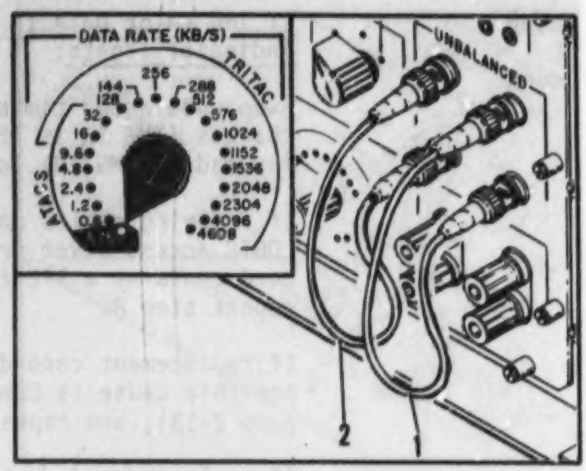
2-6. SG-1139 CHECK PROCEDURE (CONT)

Step 8 Unbalanced NRZ In

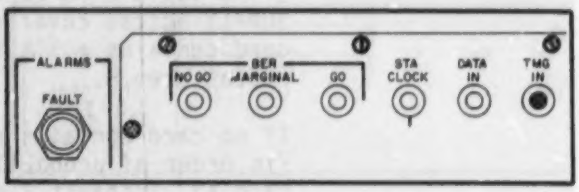
- Set controls as follows:

POWER ...... ON
TIMING ...... MASTER
DATA RATE .. 576 ATACS

Use a BNC cable (1) to connect UNBALANCED TMG OUT to UNBALANCED TMG IN:



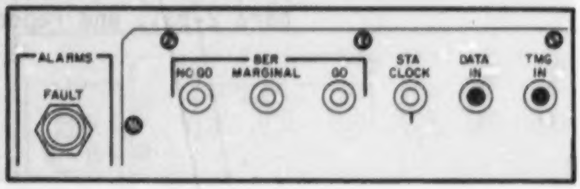
Green TMG IN indicator must light.



Continue, even if indicator does not light.

- Use a BNC cable (2) to connect UNBALANCED DATA OUT to UNBALANCED DATA IN:

Green DATA IN indicator must light. Red FAULT indicator must not light.



If both parts of this step pass, proceed to step 9. Keep cables connected.

This step checks the following:

Accessories	BNC cables
Receive 1 card ...	UNBALANCED TMG IN amplifier UNBALANCED TMG IN sensor UNBALANCED DATA IN amplifier UNBALANCED DATA IN sensor
Control Filter ...	UNBALANCED TMG OUT and IN connectors UNBALANCED TMG OUT and IN filters UNBALANCED DATA OUT and IN connectors UNBALANCED DATA OUT and IN filters

2-6. SG-1139 CHECK PROCEDURE (CONT)

Step
8
cont

If TMG IN or DATA IN indicator does not light or if FAULT indicator lights:

Swap unbalanced timing and data cables. If the lit indicator changes (TMG IN is lit instead of DATA IN or DATA IN is lit instead of TMG IN), cause is cable. Replace and repeat step 8.

If swapping cables does not change indicator that is lit, remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 8.

If replacement card does not provide proper indication, possible cause is Control Filter A8. Replace (refer to para 2-13), and repeat step 8.

If no logic card contains a lit fault indicator, remove POWER SUPPLY access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 8.

If no card contains a lit fault indicator, possible cause is (in order of probability): Receive 1 card A5, Transmit 1 card A3, Transmit 2 card A4, or Multi VDC card A1. Replace, one at a time (refer to TM 11-6625-3041-12), and repeat step 8.

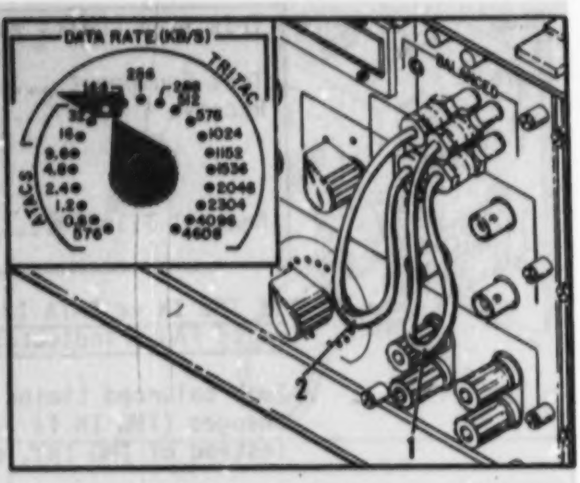
If replacement card does not provide proper indication, possible cause is Control Filter A8. Replace (refer to para 2-13), and repeat step 8.

2-6. SG-1139 CHECK PROCEDURE (CONT)

Step 9 Balanced NRZ In

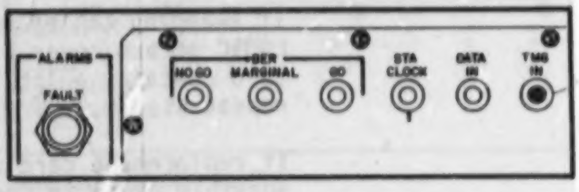
- Set controls as follows:

POWER ...... ON
TIMING ..... MASTER
DATA RATE .. 128



Use a triaxial cable (1) to connect BALANCED TMG OUT to BALANCED TMG IN:

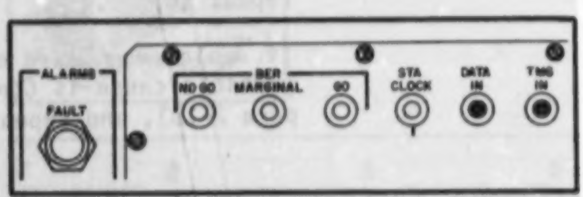
Green TMG IN indicator must light.



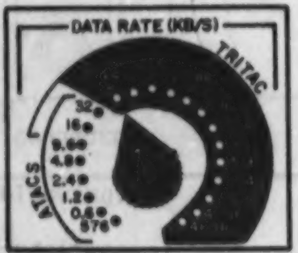
Continue, even if indicator does not light.

- Use a triaxial cable (2) to connect BALANCED DATA OUT to BALANCED DATA IN:

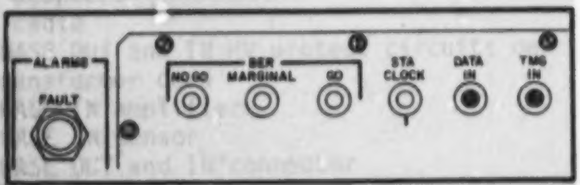
Green DATA IN indicator must light. Red FAULT indicator must not light.



- Set DATA RATE to 128 through 4608:



At each setting, TMG IN and DATA IN indicators must light.



If all parts of this step pass, proceed to step 10. Keep cables connected.

2-6. SG-1139 CHECK PROCEDURE (CONT)

Step
9
cont

This step checks the following:

Test Equipment	Triaxial cables
Receive 1 card	BALANCED TMG IN amplifier BALANCED TMG IN sensor BALANCED DATA IN amplifier BALANCED DATA IN sensor
Control Filter	BALANCED TMG OUT and IN connectors BALANCED DATA OUT and IN connectors

If TMG IN or DATA IN indicator does not light at all settings or if FAULT indicator lights at any setting:

Swap balanced timing and data cables. If the lit indicator changes (TMG IN is lit instead of DATA IN or DATA IN is lit instead of TMG IN), cause is cable. Replace and repeat step 9.

If swapping cables does not change indicator that is lit, remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 9.

If replacement card does not provide proper indication, possible cause is Control Filter A8. Replace (refer to para 2-13), and repeat step 9.

If no card contains a lit fault indicator, possible cause is Receive 1 card A5. Replace (refer to TM 11-6625-3041-12), and repeat step 9.

If replacement card does not provide proper indication, possible cause is Control Filter A8. Replace (refer to para 2-13), and repeat step 9.

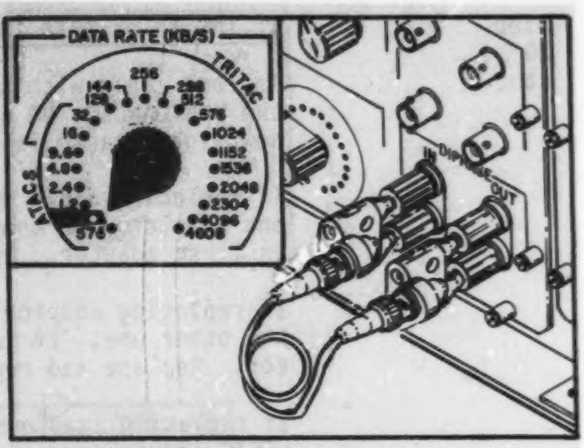
2-6. SG-1139 CHECK PROCEDURE (CONT)

Step 10 Diphase In

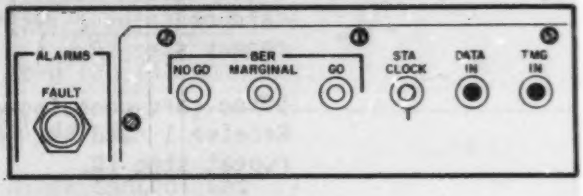
- Set controls as follows:

POWER ...... ON
TIMING ..... MASTER
DATA RATE .. 0.6

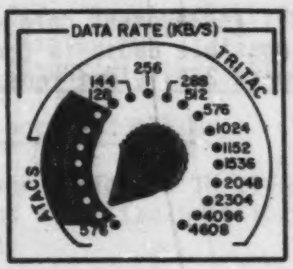
Use two BNC adapters and a BNC cable to connect DIPHASE OUT to DIPHASE IN:



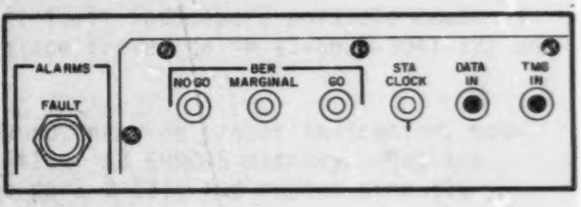
Green TMG IN and DATA IN indicators must light. Red FAULT indicator must not light.



- Set DATA RATE to 0.6 through 32:



At each setting, TMG IN and DATA IN indicators must light.



If both parts of this step pass, proceed to step 11. Keep cables connected.

This step checks the following:

Accessories	BNC adapters BNC cable
Case Assembly	DIPHASE OUT and IN HV protect circuits on transformer card
Receive 1 card ...	DIPHASE IN amplifier DIPHASE IN sensor
Control Filter ...	DIPHASE OUT and IN connector

2-6. SG-1139 CHECK PROCEDURE (CONT)

Step 10 cont

If TMG IN or DATA IN indicator does not light at all settings:

Replace cable with a known good one (such as one that connects the UNBALANCED TMG or DATA connectors together). If indicators now light, cause is original cable. Replace and repeat step 10.

If replacing cable does not provide proper indication, replace one adapter with another one. If indicators now light, cause is first adapter. Replace and repeat step 10.

If replacing adapter does not provide proper indication, replace the other one. If indicators now light, cause is second adapter. Replace and repeat step 10.

If replacing adapters does not provide proper indication, remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 10.

If no card contains a lit fault indicator, possible cause is Receive 1 card A5. Replace (refer to TM 11-6625-3041-12), and repeat step 10.

If replacement card does not provide proper indication, possible cause is Control Filter A8. Replace (refer to para 2-13), and repeat step 10.

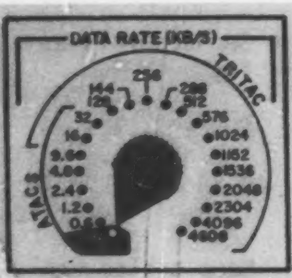
-6. SG-1139 CHECK PROCEDURE (CONT)

Step 11 Errors Display

- Set controls as follows:

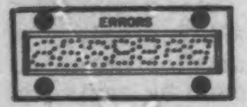
POWER .... ON
TIMING ..... MASTER

DATA RATE .. 576
ATACS



Keep cables connected. Press and hold LAMP TEST pushbutton:

ERRORS display must read all 8s. If it does, release LAMP TEST pushbutton and proceed to step 12.



Keep cables connected.

This step checks the following:

Transmit 2 card ..... Clock Control Gen
Error Counter (all 8s function)
Display Mux
Control Filter ...... ERRORS display (all 8s function)

If ERRORS display does not read all 8s:

Remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 11.

If no card contains a lit fault indicator, possible cause is Transmit 2 card A4. Replace (refer to TM 11-6625-3041-12) and repeat step 11.

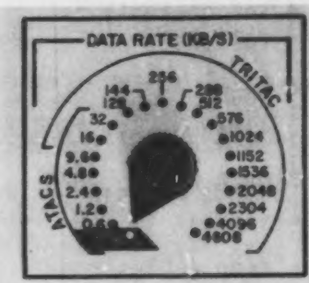
If replacement card does not provide proper indication, possible cause is Control Filter A8 ERRORS display. Replace control filter (refer to para 2-13), and repeat step 11.

2-6. **SG-1139 CHECK PROCEDURE** (CONT)

Step 12 Error Generation and Detection

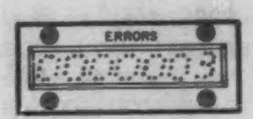
- Set controls as follows:

POWER ...... ON
TIMING ..... MASTER
DATA RATE .. 576 ATACS



Keep cables connected. Press SINGLE ERROR pushbutton several times:

ERRORS display must increase count by one each time SINGLE ERROR is pressed. If step passes, proceed to step 13. Keep cables connected.



This step checks the following:

Transmit 1 card ...	Single Error Inject
Transmit 2 card ...	Error Counter (count function)
Receive 1 card	PR GEN Error Det
Control Filter	SINGLE ERROR pushbutton ERRORS display (count function)

If ERRORS display does not increase count:

Remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 12.

If no card contains a lit fault indicator, possible cause is (in order of probability): Receiver 1 card A5, Transmit 2 card A4, or Transmit 1 card A3. Replace, one at a time (refer to TM 11-6625-3041-12), and repeat step 12.

If replacement card does not provide proper indication, possible cause is Control Filter A8. Replace (refer to para 2-13), and repeat step 12.

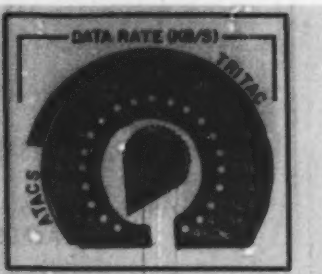
2-6. SG-1139 CHECK PROCEDURE (CONT)

Step 13 Reset and Error Count

- Set controls as follows:

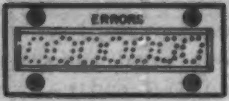
POWER .... ON
TIMING ... MASTER

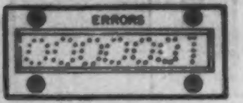
Keep cables connected. Set DATA RATE to 576 ATACS through 4608 (all settings).



At each setting, press RESET DISPLAY then press SINGLE ERROR:

Errors display must read zero when RESET is pressed and must increase count by one each time SINGLE ERROR is pressed.





If this step passes, proceed to step 14. Keep cables connected.

This step checks the following:

Control Filter	ERRORS display (set 0s function)
Transmit 2 card ...	Error Counter (set 0s function)
Receive 2 card	BER Control (Error Counter set 0s)

If ERRORS display digits do not all change to zero:

Remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 13.

If no card contains a lit fault indicator, possible cause is (in order of probability): Receive 2 card A6 or Transmit 2 card A4. Replace, one at a time (refer to TM 11-6625-3041-12), and repeat step 13.

If replacement card does not provide proper indication, possible cause is Control Filter A8. Replace (refer to para 2-13), and repeat step 13.

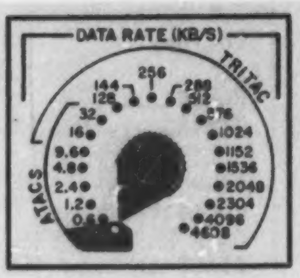
2-6. **SG-1139 CHECK PROCEDURE** (CONT)

Step 14 Unbalanced NRZ BER

- Set controls as follows:

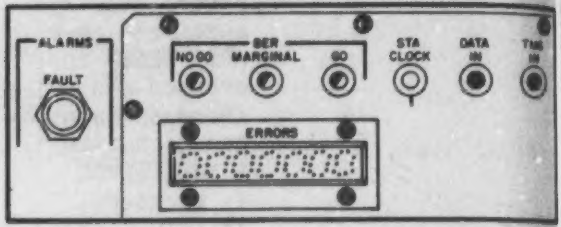
POWER ...... ON
TIMING ..... MASTER

DATA RATE .. 576 ATACS

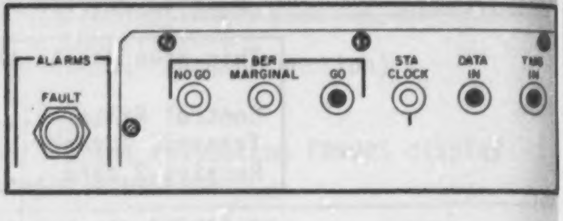


Keep cables connected. Press RESET DISPLAY:

Errors display must read zero and BER indicators must be blinking.



After 1 to 2 seconds, BER indicators must stop blinking and green GO indicator must light.



If this step passes, proceed to step 15. Keep cables connected.

This step checks the following:

Receive 2 card ... BER Control
BER Duration Counter 10^5 and 10^6 outputs
Red Error Count 100 output
Yellow Error Count 10 output
Green Circuit

If BER indications are improper:

Remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 14.

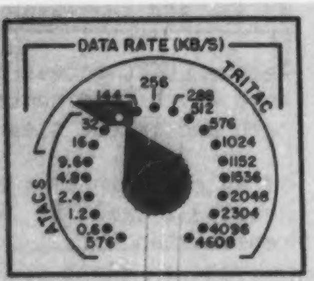
If no card contains a lit fault indicator, possible cause is Receive 2 card A6. Replace (refer to TM 11-6625-3041-12), and repeat step 14.

-6. SG-1139 CHECK PROCEDURE (CONT)

Step 15 Balanced NRZ BER

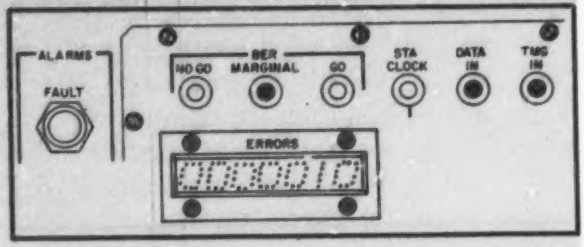
- Set controls as follows:

POWER ...... ON
TIMING ..... MASTER
DATA RATE .. 128



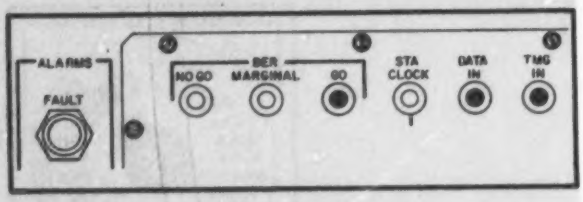
Keep cables connected. Press RESET DISPLAY, then press SINGLE ERROR rapidly 10 times (all presses must be done within 6 seconds):

BER indicators must blink. Then, after 7 to 8 seconds, yellow marginal indicator must light.



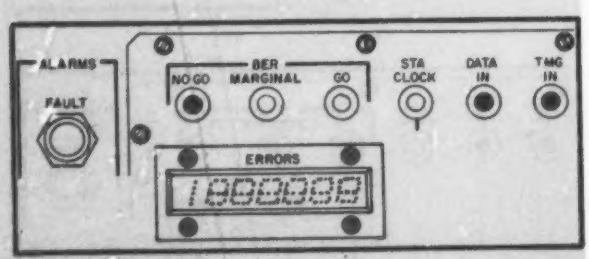
- Wait 7 to 8 seconds

Green GO indicator must light.



- Disconnect BALANCED DATA IN from BALANCED DATA OUT:

ERRORS display must increase count rapidly. Red NO GO indicator must light.



If all parts of this step pass, proceed to step 16. Keep remaining cables connected.

This step checks the following:

Receive 2 card ... Red circuit
Yellow circuit

2-6. SG-1139 CHECK PROCEDURE (CONT)

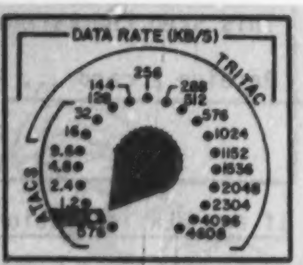
Step	
15 cont	If any BER indicator is improper: Remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 15. If no card contains a lit fault indicator, possible cause is Receive 1 card A6. Replace (refer to TM 11-6625-3041-12), and repeat step 15.

2-6. SG-1139 CHECK PROCEDURE (CONT)

Step 16 Diphase BER

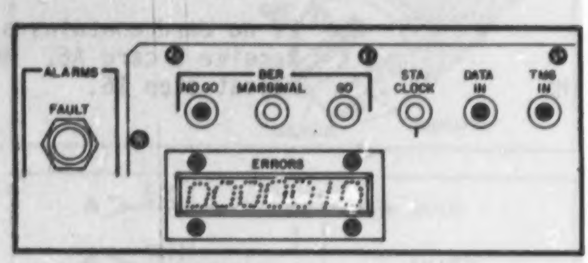
- Set controls as follows:

  POWER ...... ON
  TIMING ..... MASTER
  DATA RATE .. 0.6

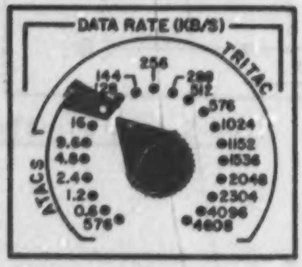


  Keep remaining cables connected. Press RESET DISPLAY, then press SINGLE ERROR rapidly 10 times (all presses must be done within 15 seconds):

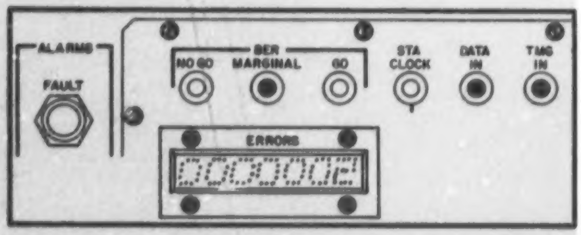
  Red NO GO indicator must light.



- Set DATA RATE to 32. Press RESET DISPLAY, then press SINGLE ERROR rapidly two times (all presses must be done within 5 seconds):

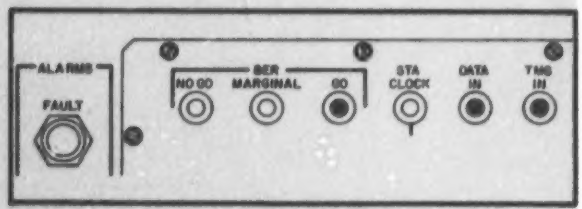


  BER indicators must blink. Then, after 6 to 7 seconds, yellow MARGINAL indicator must light.



- Wait 6 to 7 seconds:

  Green GO indicator must light.



If all parts of this step pass, disconnect remaining cables--test complete.

2-6. SG-1139 CHECK PROCEDURE (CONT)

Step
16
cont

> This step checks the following:
>
> Receive 2 card ... BER Duration Counter 10^4 and 2×10^5
> outputs
> Red Error Count 10 output
> Yellow Error Count 2 output

If any BER indication is improper:

Remove LOGIC access cover (refer to TM 11-6625-3041-12) and note which card contains a lit fault indicator. Replace that card and repeat step 16.

If no card contains a lit fault indicator, possible cause is Receive 2 card A6. Replace (refer to TM 11-6625-3041-12), and repeat step 16.

END

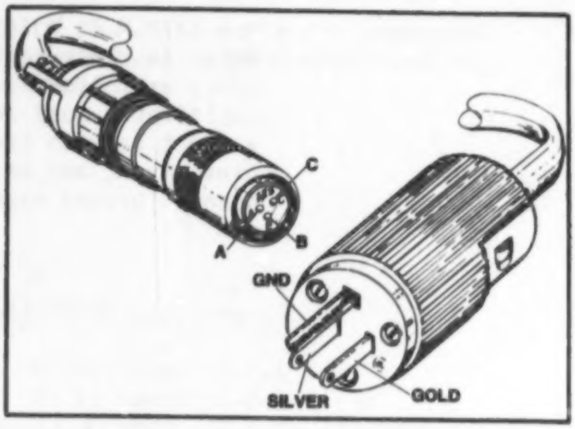
2-7. POWER CABLE CHECK PROCEDURE

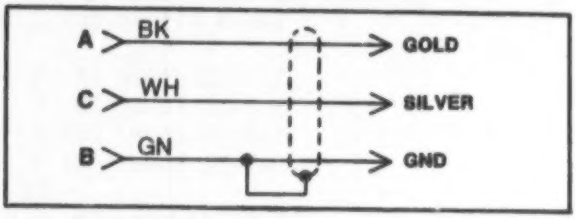
Equipment Required	AN/PSM-45 Multimeter, Digital

Visual

- Visually inspect for defects such as loose or damaged connectors, open insulation, and frayed wires.
- Use AN/PSM-45 Multimeter to check continuity as follows:

From	To	Reading
A	GOLD	Short
A	SILVER	Open
A	GND	Open
C	SILVER	Short
C	GND	Open
B	GND	Short





If defective, repair (refer to para 2-15).

2-8. INTERFACE BOX CHECK PROCEDURE

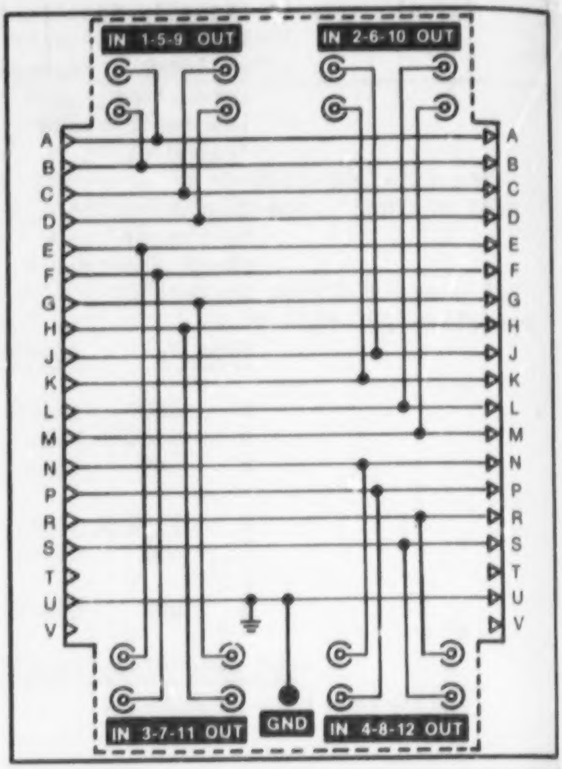
Equipment Required	AN/PSM-45 Multimeter, Digital

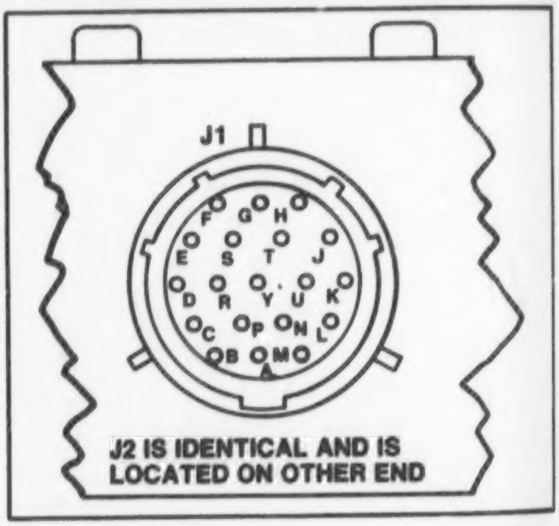
Procedure

- Use AN/PSM-45 Multimeter to check continuity as follows (multimeter must read a short between the pins given, and an open to ground except pin U):

From Banana Jack		To J1	To J2
1-5-9	upper IN	A	A
1-5-9	lower IN	B	B
1-5-9	upper OUT	C	C
1-5-9	lower OUT	D	D
3-7-11	upper IN	E	E
3-7-11	lower IN	F	F
3-7-11	upper OUT	G	G
3-7-11	lower OUT	H	H
2-6-10	upper IN	J	J
2-6-10	lower IN	K	K
2-6-10	upper OUT	L	L
2-6-10	lower OUT	M	M
4-8-12	upper IN	N	N
4-8-12	lower OUT	P	P
4-8-12	upper IN	R	R
4-8-12	lower OUT	S	S
Short to ground		U	U

If defective, repair (refer to para 2-17).





Section IV

PREVENTIVE MAINTENANCE CHECKS AND SERVICES

2-9. MONTHLY PREVENTIVE MAINTENANCE

Refer to monthly preventive maintenance procedure in TM 11-6625-3041-12, Operator's and Organizational Maintenance Manual.

Section V

TROUBLESHOOTING

2-10. TROUBLESHOOTING

Refer to troubleshooting information in TM 11-6625-3041-12, Operator's and Organizational Maintenance Manual.

Section VI

MAINTENANCE PROCEDURES

2-11. REFERENCE MAINTENANCE PROCEDURES

Refer to TM 11-6625-3041-12, Operator's and Organizational Maintenance Manual, for the following procedures:

Lamp Replacement
Logic Card Replacement
Power Supply Card Replacement
Power Input Cover Replacement

2-12. KNOB REPLACEMENT

Both the TIMING and DATA RATE knobs are replaceable.

Tools and Materials Required

TK-101/G Tool Kit , Electronic Equipment for:

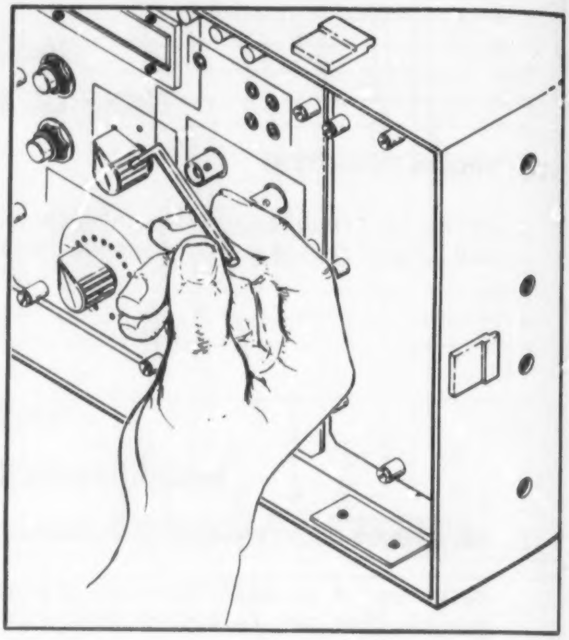
0.050-in. hex wrench

Primer (item 1, Appendix B).

Sealing compound (item 2, Appendix B).

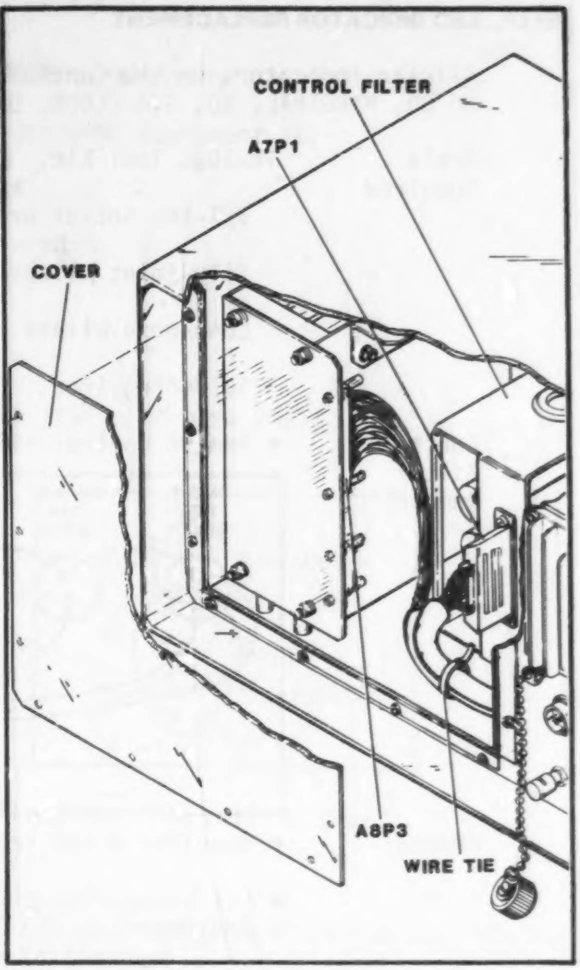
Removal

- Note position at which knob is set.
- Use 0.050-in. hex wrench to loosen the two set screws in the knob.
- Remove knob.
- Use 0.050-in. hex wrench to remove the two set screws from the new knob.
- Apply a drop of primer to each set screw.
- Apply a drop of sealing compound to each set screw.



- Use 0.050-in. hex wrench to reinstall the set screws in the new knob.
- Install new knob on shaft in same position as knob that was removed.
- Use 0.050-in. hex wrench to tighten the two set screws that secure knob to shaft.

CONTROL FILTER REPLACEMENT



Tools Required

- TK-101/G Tool Kit, Electronic Equipment for:
  - 1/4 in. socket wrench
  - Flat-tip screwdriver
  - Cross-tip screwdriver
  - Diagonal pliers

Removal

- Set power to off.
- Use a cross-tip screwdriver to remove the 14 screws that secure the cover to the rear panel. Remove cover.
- Use diagonal pliers to remove wire tie on cables to A7P1 and A8P3.
- Use a flat-tip screwdriver to loosen the two screws that secure A7P1 to the back of the Control Filter. Disconnect A7P1.
- Use a 1/4-in. socket wrench (or flat-tip screwdriver) to loosen the 12 captive screws on front panel of Control Filter. Pull out Control Filter.

Replacement

- Insert Control Filter into front-panel opening. Use a 1/4-in. socket wrench (or flat-tip screwdriver) to tighten the 12 captive screws on front panel of Control Filter.
- Reconnect A8P3 to the logic backplane. Use a flat-tip screwdriver to secure A8P3 to the logic backplane.
- Reconnect A7P1 to the back of the Control Filter. Use a flat-tip screwdriver to secure A7P1 to the Control Filter.
- Install a wire tie on cables to A7P1 and A8P3.
- Reinstall the cover on the rear panel. Use a cross-tip screwdriver to tighten the 14 screws that secure the cover to the rear panel.

2-14. LED INDICATOR REPLACEMENT

All six indicators on the Control Filter are replaceable and include the NO GO, MARGINAL, GO, STA CLOCK, DATA IN, and TMG IN indicators.

Tools Required

TK-101G Tool Kit , Electronic Equipment for:

1/4-in. socket wrench

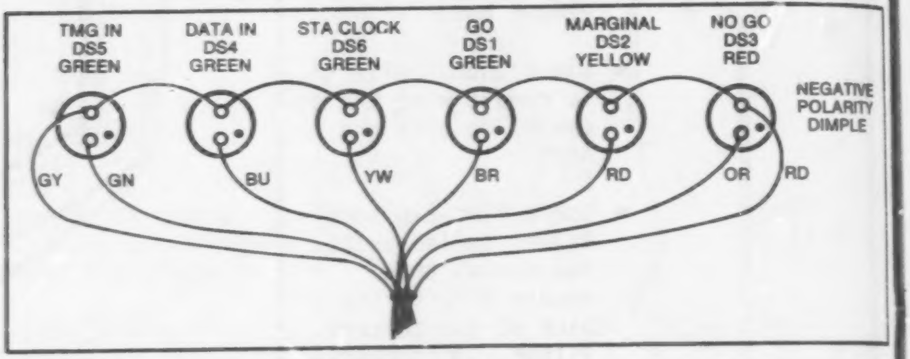
Slip-joint pliers

Long-nose pliers

Soldering iron

Control Filter Removal

- Remove Control Filter (refer to para 2-13).



Removal

- Unsolder wires from back of indicator.
- Use slip-joint pliers to remove knurled nut from front of indicator.
- Remove indicator by pulling out from back of panel.

Replacement

- Insert new indicator.
- Reinstall washer and nut on front of indicator and use slip-joint pliers to tighten.
- Resolder wires to back of indicator.

2-15. PUSHBUTTON REPLACEMENT

Both the RESET DISPLAY and SINGLE ERROR pushbuttons are replaceable.

Tools Required — TK-101/G Tool Kit , Electronic Equipment for:

1/4-in. socket wrench

Adjustable open-end wrench

Long-nose pliers

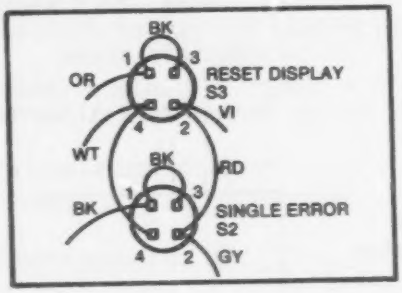
Soldering iron

Control Filter Removal

- Remove Control Filter (refer to para 2-13).

Removal

- Unsolder wires from back of pushbutton switch.
- Use adjustable open-end wrench to remove nut from front of switch.



- Remove switch by pulling out from back of panel.

Replacement

- Insert new switch.
- Reinstall washer and nut on front of switch and use adjustable open-end wrench to tighten.
- Resolder wires to back of switch.

2-16. POWER CABLE REPAIR

Tools and Material Required

TK-101G Tool Kit , Electronic Equipment for:

- Slip-joint pliers (2 ea)
- Diagonal cutting pliers
- Flat-tip screwdriver
- Solder

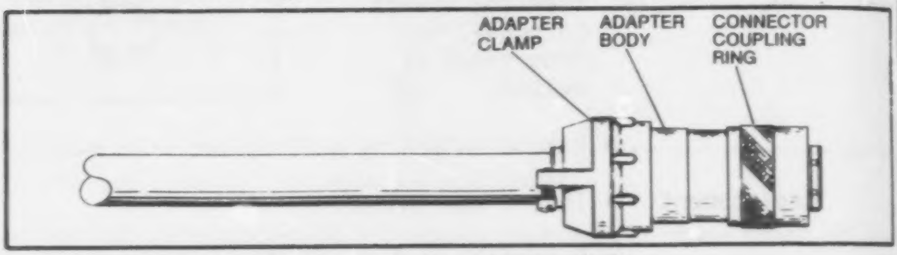
PRC-350C Bench Top Repair Facility for:

- Soldering iron
- Thermal wire stripper
- Hot-air probe

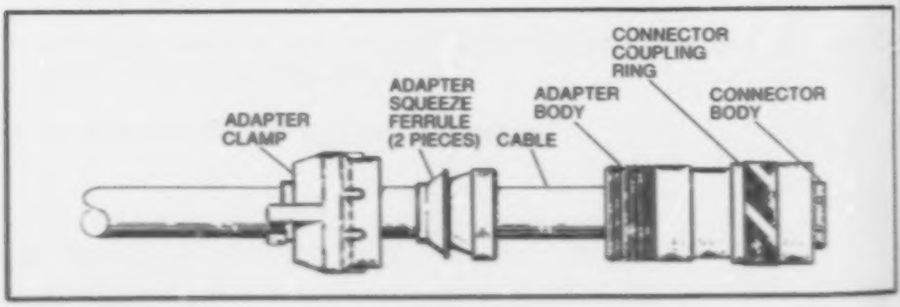
Heat-shrink sleeving, 0.187 in. ID (item 3, Appendix B)

Heat-shrink sleeving, 0.125 in. ID (item 4, Appendix B)

Female Connector Disassembly

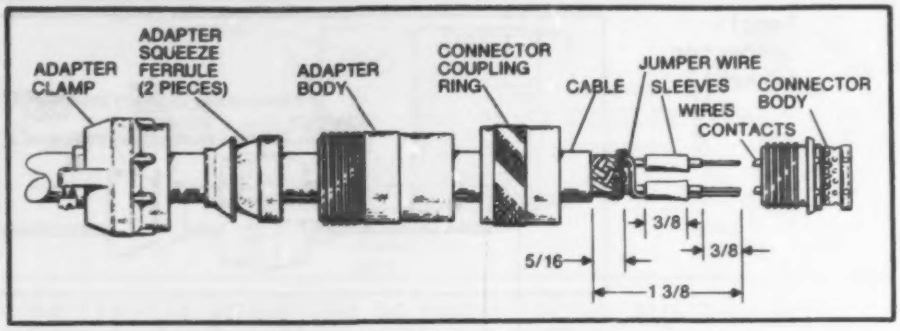


- Use slip-joint pliers to hold adapter body.
- Use another pair of slip-joint pliers to turn adapter clamp counterclockwise to remove from adapter body.



- Move adapter clamp and adapter squeeze ferrule back on cable 2 or 3 inches.
- Use slip-joint pliers to hold connector body.
- Use another pair of slip-joint pliers to turn adapter body counterclockwise to remove from connector body.

2-16. POWER CABLE REPAIR (CONT)



- Move adapter body and connector coupling ring back on cable 2 or 3 inches.

- Use diagonal cutting pliers to cut off insulating sleeves.

Female Connector Broken Wires

All wires must be the same length. To repair a broken wire, it is necessary to unsolder all wires and cut to the same length.

- Temporarily tag all wires for pin connections.

- Unsolder all wires from contacts.

- Cut ends of wires so they are the same length.

- Strip wires 3/8 in. and tin.

- Cut and remove cable insulation at a point 1 3/8 in. back from ends of wires.

- Add new sleeves.

- Solder wires into contacts.

- Move insulating sleeves back into position over contacts.

- Cut shield 7/16 in. long.

- Fan shield and jumper wire and mesh together.

For assembly, see FemaleConnector Assembly below.

Female Connector Replacement

- Unsolder all wires from contacts.

- Replace damaged or mising connector components.

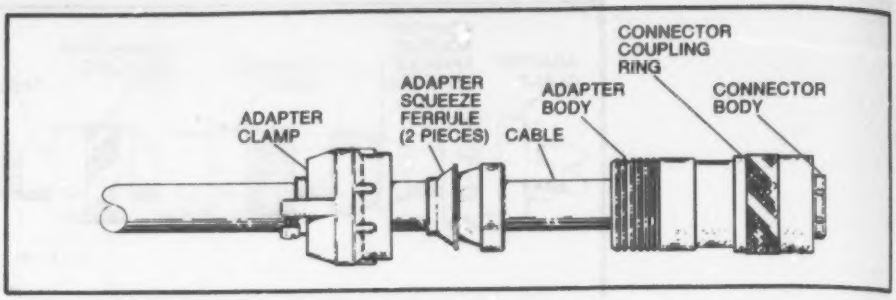
- Add new sleeves.

- Solder wires into contcts.

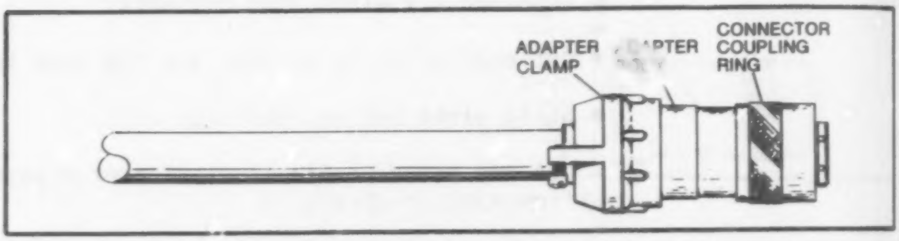
- Move insulating sleeve back into position over contacts.

2-16. POWER CABLE REPAIR (CONT)

Female Connector Assembly



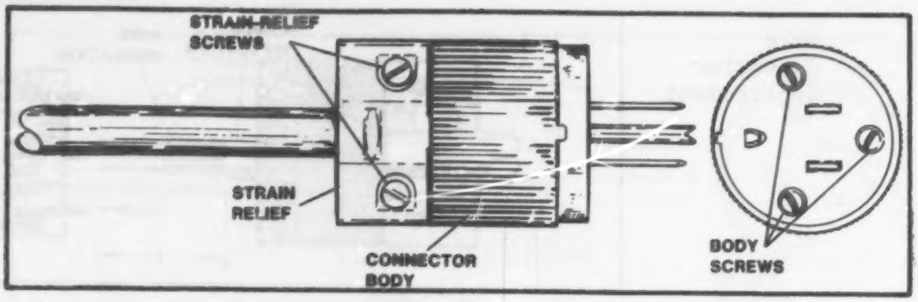
- Move connector coupling ring back over connector body.
- Move adapter body back over connector body and turn clockwise handtight.
- Use slip-joint pliers to hold connector body.
- Use another pair of slip-joint pliers to turn adapter body clockwise to secure to connector body.
- Move adapter squeeze ferrule over cable shield and jumper wire, against adapter body.



- Move adapter clamp over adapter body and turn clockwise handtight.
- Use slip-joint pliers to hold adapter body.
- Use another pair of slip-joint pliers to turn adapter clamp clockwise to secure to adapter body.

2-16. POWER CABLE REPAIR (CONT)

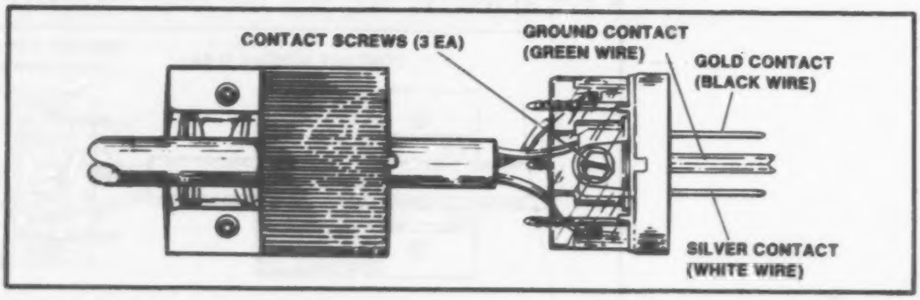
Male Connector Disassembly



- Use flat-tip screwdriver to remove the two strain-relief screws.
- Remove strain-relief cover.
- Use flat-tip screwdriver to remove the three body screws.
- Slip strain-relief back on cable 3 or 4 inches.

Male Connector Broken Wires

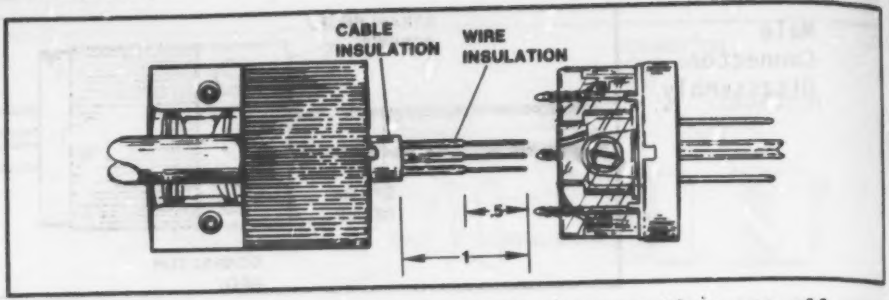
All wires must be the same length. To repair a broken wire, it is necessary to cut all wires to the same length.


CONTACT SCREWS (3 EA)
GROUND CONTACT (GREEN WIRE)
GOLD CONTACT (BLACK WIRE)
SILVER CONTACT (WHITE WIRE)

- Use flat-tip screwdriver to loosen all three contact screws.
- Pull wires out of contacts.

2-16. POWER CABLE REPAIR (CONT)

Male
Connector
Replacement



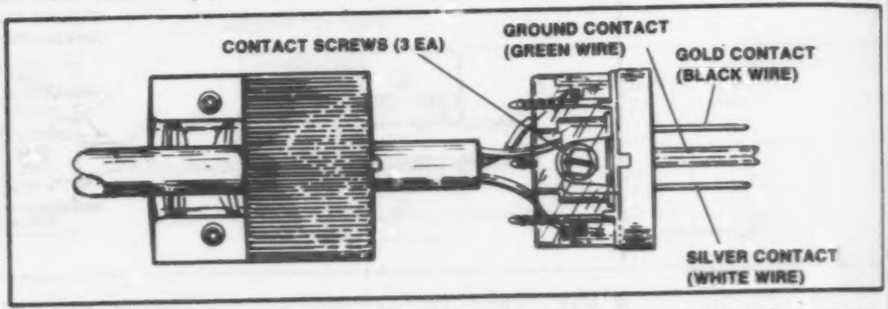
- Use diagonal pliers to cut ends of wires so they are all the same length.

- Strip cable insulation so that it is 1 inch back from enc of wires.

- Strip wire insulation so that it is 0.5 inch back from end of wires.

- Twist end of each wire.

- For assembly, see Male Connector Assembly below.

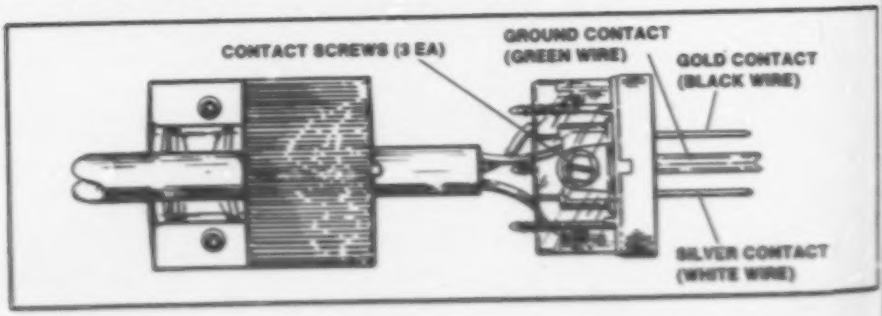

CONTACT SCREWS (3 EA)
GROUND CONTACT (GREEN WIRE)
GOLD CONTACT (BLACK WIRE)
SILVER CONTACT (WHITE WIRE)

- Use flat-tip screwdriver to loosen all three contact scrws.

- Pull wires out of contacts.

- Replace damaged or missing connector components.

Male
Connector
Assembly

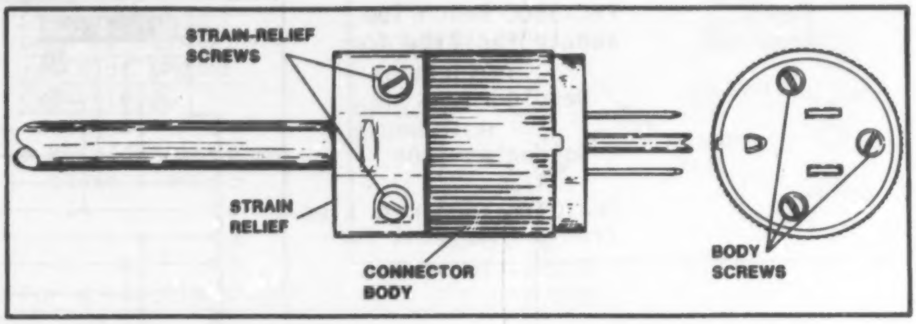

CONTACT SCREWS (3 EA)
GROUND CONTACT (GREEN WIRE)
GOLD CONTACT (BLACK WIRE)
SILVER CONTACT (WHITE WIRE)

- Insert wires in contacts.

- Use flat-tip screwdriver to tighten all three contact screws.

2-16. POWER CABLE REPAIR (CONT)

Male Connector Assembly (cont)



- Slip strain relief up to connector body.
- Reinstall the three body screws and use flat-tip screwdriver to tighten.
- Slip strain relief up to connector body.
- Reinstall the strain-relief cover.
- Reinstall the strain-relief screws and use flat-tip screwdriver to tighten.

2-17. INTERFACE BOX REPAIR

Tools Required

PRC-350C Bench Top Repair Facility for:

- Desolderer
- Soldering iron

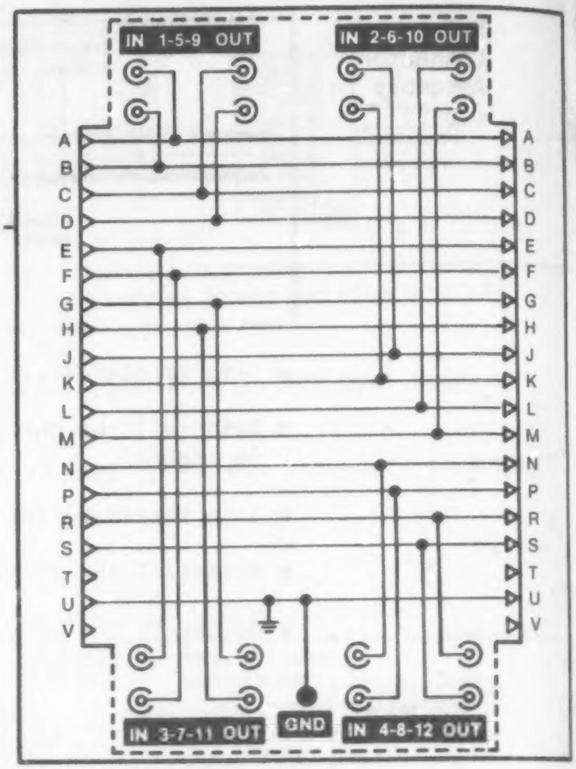
TK-101/G Tool Kit, Electronic Equipment for:

- Cross-tip screwdriver
- 3/8-in. socket wrench
- Slip-joint pliers
- Diagonal cutting pliers
- Adjustable open-end wrench

RX116-7 extractor

RTM16-2 insertion tool

M22520/1-01 crimping tool with M22520/1-02 locator

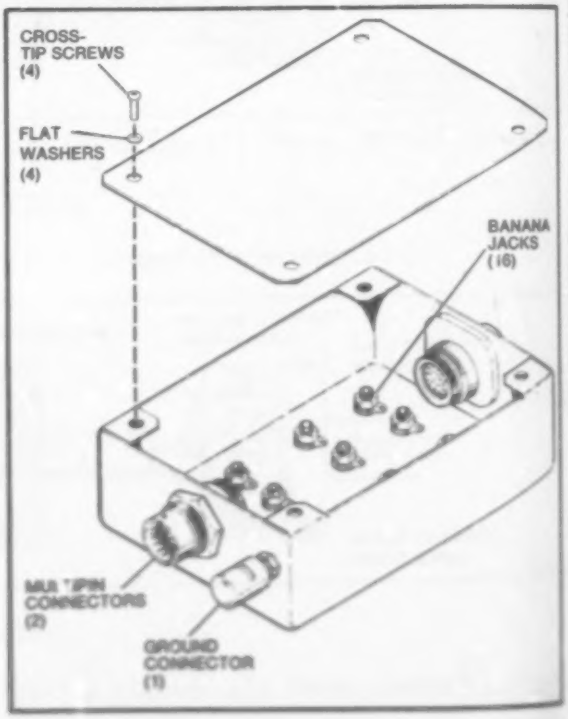


Access

- Use cross-tip screwdriver to remove four screws with flat washers that secure bottom cover.
- Remove cover.

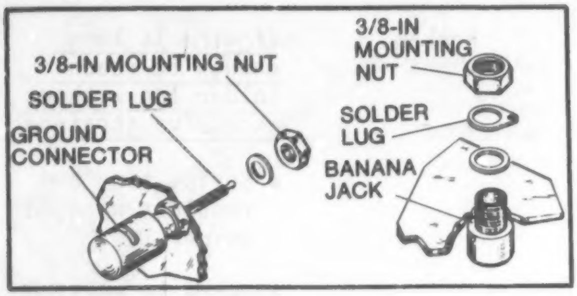
Visual Inspection

- Visually inspect for defects such as open connections, broken wires, and loose or damaged connectors.

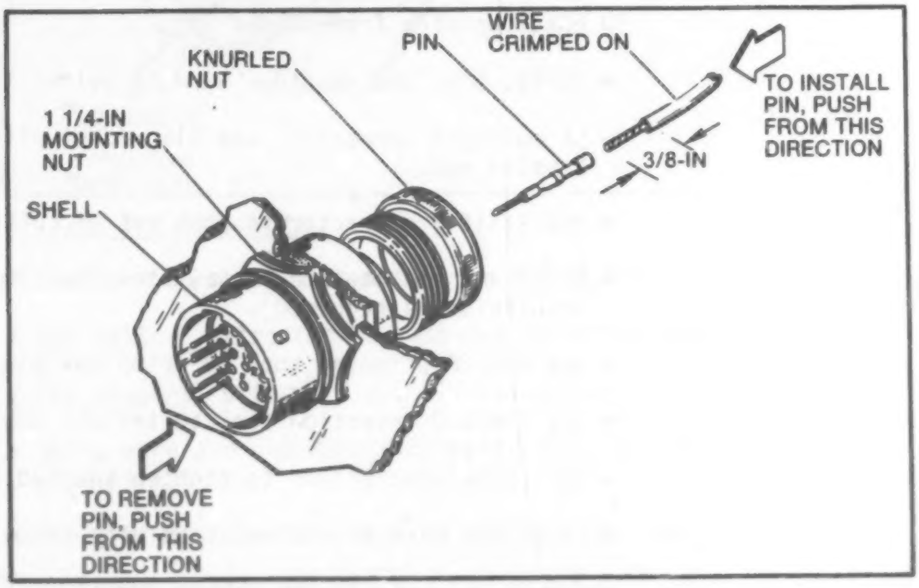


-17. INTERFACE BOX REPAIR (CONT)

Open Connections	For connections open at banana jacks or ground connector: - Resolder any open connections.

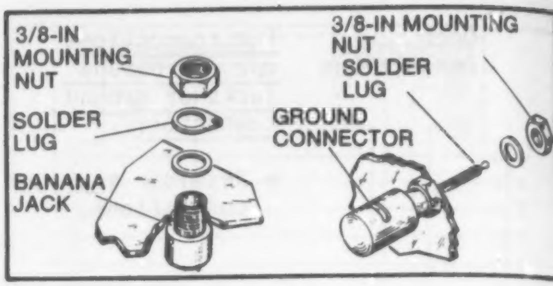


For connections open at multipin connector:


KNURLED NUT
PIN
WIRE CRIMPED ON
TO INSTALL PIN, PUSH FROM THIS DIRECTION
1 1/4-IN MOUNTING NUT
3/8-IN
SHELL
TO REMOVE PIN, PUSH FROM THIS DIRECTION

- Use slip-joint pliers to loosen knurled nut.
- Tag wires for later replacement.
- Use RX116-7 extractor to push out pin with open connection.
- Use diagonal cutting pliers to cut off pin from wire.
- Strip wire and use M22520 crimping tool to crimp new pin onto wire.
- Use RTM16-2 insertion tool to install new pin.
- Use slip-joint pliers to tighten knurled nut.

2-17. INTERFACE BOX REPAIR (CONT)



Broken Wires

If wire is long enough to reach solder lug without excessive strain:

- Strip, tin, and resolder wire to solder lug.

If wire is not long enough to reach solder lug without excessive strain:

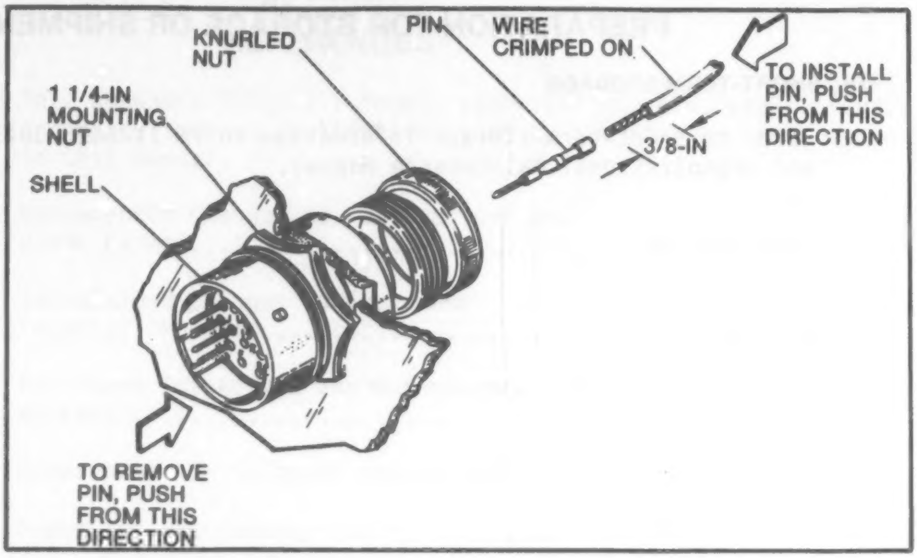
- Unsolder wire from solder lug.
- Strip, tin, and resolder wire to solder lug.
- At multipin connector, use slip-joint pliers to loosen knurled nut.
- Use RX116-7 extractor to push out pin with broken wire.
- Strip and tin one end of new wire (No. 20 with white or black insulation as required).
- Use M22520 crimping tool to crimp new pin onto wire.
- Use RTM16-2 insertion tool to install new pin.
- Use slip-joint pliers to tighten knurled nut.
- Twist new wire around existing wire in pair.
- Cut new wire to length, strip and tin loose end.
- Solder new wire to solder lug.

Defective Banana Jack or Ground Connector

- Unsolder wire from solder lug.
- Use 3/8-in. socket wrench to remove mounting nut.
- Remove connector and replace with a new one.
- Reinstall mounting nut and use 3/8-in. socket wrench to secur

2-17. INTERFACE BOX REPAIR (CONT)

Defective Multipin Connector


KNURLED NUT
PIN
WIRE CRIMPED ON
TO INSTALL PIN, PUSH FROM THIS DIRECTION
1 1/4-IN MOUNTING NUT
3/8-IN
SHELL
TO REMOVE PIN, PUSH FROM THIS DIRECTION

If pins are defective:

- Use hand or slip-joint pliers to loosen knurled nut.
- Use RX116-7 extractor to push out defective pin.
- Use diagonal pliers to cut off defective pin from wire.
- Strip wire and use M22520 crimping tool to crimp new pin onto wire.
- Use RTM16-2 insertion tool to install new pin.
- Use hand or slip-joint pliers to tighten knurled nut.

If shell is defective:

- Use hand or slip-joint pliers to loosen knurled nut.
- Use RX116-7 extractor to push out all 19 pins. Record locations of pins for later reinsertion.
- Use 1 1/4-in. wrench or slip-joint pliers to remove mounting nut.
- Remove multipin connector shell.
- Install new connector shell.
- Install mounting nut and use 1 1/4-in. wrench or slip-joint pliers to tighten.
- Use RTM16-2 insertion tool to push in all 19 pins.
- Use hand or slip-joint pliers to tighten knurled nut.

Section VII .

PREPARATION FOR STORAGE OR SHIPMENT

2-18. SHORT-TERM STORAGE

Refer to short-term storage information in TM 11-6625-3041-12, Operator's and Organizational Maintenance Manual.

Appendix A

REFERENCES

A-1 Scope

This appendix lists all forms, technical manuals, regulations, and miscellaneous publications used by the Army and referenced in this manual.

A-2	Forms	Recommended Changes to Publications and Blank Forms	DA Form 2028
		Recommended Changes to Equipment Technical Manuals	DA Form 2028-2
		Equipment Inspection and Maintenance Worksheet	DA Form 2404
		Discrepancy in Shipment Report (DISREP)	SF 361
		Report of Discrepancy (ROD)	SF 364
		Quality Deficiency Report	SF 368
A-3	Technical Manuals	First Aid for Soldiers	FM 21-11
		Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command)	TM 750-244-2
		Digital Data Generator SG-1139/G Operator's and Organizational Maintenance Manual	TM 11-6625-3041-12
		Digital Data Generator SG-1139/G Organizational Maintenance Repair Parts and Special Tools Lists	TM 11-6625-3041-20P
		Digital Data Generator SG-1139/G General Support Maintenance Repair Parts and Special Tools Lists	TM 11-6625-3041-30P
A-4	Regulations	Reporting of Transportation Discrepancies in Shipments	AR 55-38
		Reporting of Item and Packaging Discrepancies	AR 735-11-2

best copy available

Appendix A (CONT)

REFERENCES (CONT)

A-5	Miscellaneous Publications	Expendable Items (Except Medical, Class V, Repair Parts, and Heraldic Items)	CTA 50-970
		Consolidated Index of Army Publications and Blank Forms	DA Pam 310-1
		The Army Maintenance Management System (TAMMS)	DA Pam 738-750
		Federal Supply Code for Manufacturers (FSCM)	SB 708-41/42

Appendix B

EXPENDABLE SUPPLIES AND MATERIALS LIST

SECTION I. INTRODUCTION

B-1 Scope

This appendix lists expendable supplies and materials you will need to operate and maintain the SG-1139/G. These items are authorized to you by CTA 50-970, Expendable Items (Except Medical, Class V, Repair Parts, and Heraldic Items).

B-2 Explanation of Columns

a. Column 1, Item No. This number is assigned to the entry in the listing and is referenced in the narrative instructions to identify the material (e.g., "Use sealing compound, item 2 Appendix B").

b. Column 2, Level. This column identifies the lowest level of maintenance that requires the listed item.

C - Operator/Crew
O - Organizational Maintenance
F - Direct Support Maintenance
H - General Support Maintenance

c. Column 3, National Stock Number. This is the National stock number assigned to the item; use it to request or requisition the item.

d. Column 4, Description. Indicates the Federal item name and, if required, a description to identify the item. The last line for each item indicates the Federal Supply Code for Manufacturer (FSCM) in parentheses followed by the part number.

e. Column 5, Unit of Measure (U/M). Indicates the measure used in performing the actual maintenance function. This measure is expressed by a two-character alphabetical abbreviation (e.g., ea, in., pr). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy your requirements.

SECTION II. EXPENDABLE SUPPLIES AND MATERIALS LIST

(1) Item No.	(2) Level	(3) National Stock No.	(4) Description	(5 U/
1	H	8030-00-963-0930	Primer, grade T, MIL-S-22473	oz
2	H	8030-00-081-2328	Sealing compound, grade AA, MIL-S-22473	oz
3	H	5970-00-954-1622	Insulation sleeving, electrical, heat shrink, 0.187 in. ID before shrink (81349) M23053/5-105-0	ft
4	H	5970-00-812-2969	Insulation sleeving, electrical, heat shrink, 0.125 in. ID before shrink (81349) M23053/5-104-0	ft

GLOSSARY

Asynchronous	Independent. Data source (SG-1139) and path under test have independent timing.
Bit error rate (BER)	Number of bits in error per total bits.
Balanced	A path in which two wires are used, each of the same amplitude with respect to ground but of opposite polarity.
Clock	A signal or circuit used to achieve synchronization between various signals and equipments.
Channel	A direct path of electrical communication.
Code	A method of preparing information for electrical transmission (e.g., diphase, NRZ).
Diphase	A code in which a change in level occurs at the start of every bit period and in which a logic 0 is a second change in level one-half bit period later. Logic 1 is no transition at the start of the bit period.
Data	Information.
Data rate	Number of bits per time, usually given in thousands of bits per second (kb/s).
Duplex	A communications path in which information can be both transmitted and received at the same time.
Error	A received bit that is opposite to that transmitted (e.g., 0 when it should have been 1, or 1 when it should have been 0).
End-to-end	From one end of a path to the other.
Family	A class of signal with specific characteristics (e.g., unbalanced NRZ, diphase, balanced NRZ).
Fault	Malfunction, failure.
Group	A path that contains more than one channel.
Inhibit	Prevent an action from taking place.
Inverted	Reversed polarity.
Line-to-ground	Measured from one wire to ground.
Line-to-line	Measured from one wire to the other.
Loopback	From one end of a path to the other, then back again.

GLOSSARY (cont)

Nonreturn to zero	A code in which logic 1 is high level and logic 0 is low level.
Off line	Not part of an active transmission path.
Pseudorandom	Not totally random.
Station clock	A clock signal that originates in the station or communications system.
Synchronous	Having a regular time relationship, not independent.
Timing	Process of making synchronous or the signal used to make synchronous.
Triaxial	A type of connector that contains two contacts for a balanced signal, plus a ground contact.
Transient	Momentary or a signal with a brief change or surge in amplitude.
Unbalanced	A path in which a single wire with ground return is used.

ALPHABETICAL INDEX

Page

A
- AC Input A2
  - Principles 1-26, 1-27, 1-28
  - Replacement 2-29
  - Schematic FO-4
  - Troubleshooting 2-4
- Administrative storage 1-4
- Appendixes
  - Expendable supplies and materials list B-1
  - References A-1

- Bit error rate
  - Indicator replacement 2-32
  - Principles 1-21

- Cable
  - Power, check procedure 2-27
  - Power, repair procedure 2-34
- Capabilities of equipment 1-5
- Changes to equipment technical manuals recommended, form .. i, back
- Chapter contents 1-1, 2-1
- Characteristics of equipment 1-5
- Check procedures
  - Interface box 2-28
  - Power cable 2-27
  - SG-1139/G 2-3
- Color codes FO-1
- Common tools and equipment 2-2
- Consolidated index of Army publications and blank forms ... 1-3
- Contents
  - Chapter 1-1, 2-1
  - Overall i
- Cross-reference, nomenclature 1-4

- Data, equipment
- DC supplies
  - Card replacement 2-29
  - Principles 1-26
  - Schematic FO-3, FO-4
  - Troubleshooting 2-4
- Description of equipment 1-5
- Destruction of Army materiel to prevent enemy use 1-3
- Diphase in principles 1-14
- Diphase out principles 1-7
- Documents, list of applicable 1-3, A-1

- Effective pages list C
- Electrical shock .... A
- Equipment
  - Capabilities 1-5
  - Characteristics 1-5

ALPHABETICAL INDEX (CONT)

Page

    Features 1-5
    Improvement recommendations 1-4
    Maintenance 2-29
    Nomenclature cross-reference list 1-4
    Principles of operation 1-5
    Repair procedures 2-29
    Test procedures 2-3
Error count principles 1-18
Error detection principles 1-16
Error rate, bit
    Indicator replacement 2-32
    Principles 1-21
Errors, reporting .... i, back
Expendable supplies and materials list B-1

F
Fault sensing
    Logic circuit principles 1-24
    Power supply principles 1-28
Features of equipment 1-5
First aid .... B
Foldouts FO-1
Forms
    Discrepancy in shipment report, SF-361 1-3
    Recommended changes to equipment technical publications, DA Form 2028-2 .... i, back
    Recommended changes to publications and blank forms, DA Form 2028 i
    Report of discrepancy, SF-364 1-3
    Quality deficiency report, SF-368 1-4
Forms list 1-3, A-1

G
General principles 1-5
Glossary Gloss-1

H
High-voltage warning .... A
How to use this manual iii

I
Improvement of equipment, recommendations 1-4
Indexes
    Alphabetical Index-1
    Army publications and blank forms 1-3
    Publications A-1
Indicators
    Bit error rate principles 1-21
    Bit error rate replacement 2-32
    Fault sensing 1-24, 1-28
    Input replacement 2-31
    Input sensing 1-24
    Lamp replacement 2-29
    LED replacement 2-32

ALPHABETICAL INDEX (CONT)

Page

Input
  Diphase principles 1-14
  Indicator replacement.......... 2-32
  NRZ principles 1-12
  Sensing principles 1-24
Interface Box
  Check procedure 2-28
  Repair 2-40
  Schematic FO-10

K Knob replacement 2-30

L Layout, physical 1-5
LED indicator replacement 2-32
Logic circuit
  Card replacement 2-29
  Principles 1-6
  Schematics .... FO-5 thru FO-9
  Troubleshooting 2-7

M Maintenance
  Control filter replacement 2-29
  Forms, records, and reports 1-3
  Interface box repair 2-40
  Knob replacement 2-30
  Lamp replacement 2-29
  LED indicator replacement 2-32
  Logic card replacement 2-29
  Power cable repair 2-34
  Power input cover replacement 2-29
  Power supply card replacement 2-29
  Procedures 2-29
  Pushbutton replacement.......... 2-33
Manual, scope 1-2
Manuals, technical A-1
Materials, expendable B-1
Miscellaneous publications A-1
Multi VDC card
  Principles 1-30
  Replacement 2-29
  Schematic FO-3
  Troubleshooting 2-5

N Nomenclature cross-reference 1-4
NRZ in principles 1-12
NRZ out principles 1-7
Nuclear shutdown principles 1-27

O Operation, technical principles of 1-5
Overall contents i

ALPHABETICAL INDEX (CONT)

Page

P

Parts, repair 2-2
Physical layout 1-5
Power cable
  Check procedure 2-27
  Repair 2-34
Power input cover replacement 2-29
Power supply
  Card replacement 2-29
  Principles 1-26
  Schematics FO-3, FO-4
  Troubleshooting 2-4
Preparation
  For movement 1-4, 2-44
  For storage or shipment 1-4, 2-44
Principles of operation 1-5
Publications
  Consolidated index of Army publications 1-3
  References A-1
Pushbutton replacement 2-33

R

Rate select principles 1-6
Receipt of equipment 2-2
Receive 1 card A5
  Principles 1-12, 1-24
  Replacement 2-29
  Schematic FO-7
  Troubleshooting 2-12, 2-20
Receive 2 card A6
  Principles 1-21, 1-24
  Replacement 2-29
  Schematic FO-8
  Troubleshooting 2-21
Recommended changes to equipment technical publications, DA Form 2028-2 .... i, back
Recommended changes to publications and blank forms, DA Form 2028 i
Recommending improvement 1-4
Reference maintenance procedures
  Control filter replacement........ 2-29
  Lamp replacement 2-29
  Logic card replacement 2-29
  Power input cover replacement 2-29
  Power supply card replacement 2-29
References to forms, technical manuals, regulations, and miscellaneous publications A-1
Regulations A-1
Repair parts 2-2
Repair procedures
  Interface box 2-40
  Power cable 2-34

ALPHABETICAL INDEX (CONT)

Page

Replacement procedures
    Control filter 2-29
    Knob 2-30
    Lamp 2-29
    LED indicator 2-31
    Logic card 2-29
    Power supply card 2-29
    Pushbutton 2-32
Reporting
    Equipment improvement recommendations 1-4
    Errors .... i, back
Reports
    Discrepancy in shipment, SF-361 1-3
    Of packaging and handling deficiency, SF-364 1-3
    Quality deficiency, SF-368 1-4

S

Schematics FO-2
Scope of manual 1-2
Sensing
    Logic circuit fault 1-24
    Logic circuit input 1-24
    Power supply fault 1-28
Service upon receipt 2-2
SG-1139/G check procedure 2-3
Shelter requirements 2-2
Shipment, preparation for 1-4, 2-44
Site requirements 2-2
Special tools 2-2
Storage
    Administrative 1-4
    Preparation for 1-4, 2-44
Supplies, expendable B-1
Supplies, power
    Card replacement 2-29
    Principles 1-26
    Schematics FO-3, FO-4
    Troubleshooting 2-4
Support equipment 2-2

T

Technical manuals A-1
Technical principles of operation 1-5
Test equipment required 2-2
Theory 1-5
Tools required 2-2
Transmit 1 card A3
    Principles 1-6, 1-24
    Replacement 2-29
    Schematic FO-5
    Troubleshooting 2-7, 2-20

ALPHABETICAL INDEX (CONT)

Page

Transmit 2 card A4
    Principles 1-6, 1-10, 1-18, 1-24
    Replacement 2-29
    Schematic FO-6
    Troubleshooting 2-8, 2-11, 2-19
Troubleshooting 2-29

U Using this manual iii

W Warning page .... A
Warnings
    Heavy equipment .... A
    High voltage .... A

By Order of the Secretaries of the Army and the Air Force:

JOHN A WICKHAM, JR.
General, United States Army
Chief of Staff

Official:

DONALD J. DELANDRO
Brigadier General, United States Army
The Adjutant General

Official:

EARL T. O'LOUGHLIN
General, USAF, Commander, Air Force
Logistics Command

CHARLES A. GABRIEL
General, USAF
Chief of Staff

DISTRIBUTION:

To be distributed in accordance with DA Form 12-51A-1 literature requirements for AN/TRC-151, AN/TRC-152, AN/TRC-173 and AN/TRC-174.

☆ U. S. GOVERNMENT PRINTING OFFICE : 1989 O - 235-605

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)

Commander Stateside Army Depot
Attn: AMSTA-US
Stateside, NJ 07703-5007

DATE SENT

PUBLICATION NUMBER TM 11-5840-340-12	PUBLICATION DATE 23 Jan. 1974	PUBLICATION TITLE Radar Set AN/PRC-76

BE EXACT PIN-POINT WHERE IT IS

PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
2-25	2-28			Recommend that the installation antenna alignment procedure be changed throughout to specify a 2° IFF antenna lag rather than 1°. REASON: Experience has shown that with only a 1° lag, the antenna servo system is too sensitive to wind gusting in excess of 25 knots, and has a tendency to rapidly accelerate and decelerate as it hunts, causing strain to the drive train. Hunting [illegible] minimized by adjusting the lag to 2° without degradation of operation.
3-10	3-3		3-1	Item [illegible] Function column. Change "2 dB" to "3 dB." REASON: The adjustment procedure the TRANS POWER FAULT indicator calls for a 3 dB (500 watts) adjustment to light the TRANS POWER FAULT indicator.
5-6	5-8			Add new step f.1 to read, "Replace cover plate removed in step e.1, above." REASON: To replace the cover plate.
		F03		Zone C 3. On J1-2, change "+24 VDC" to "+5 VDC." REASON: This is the output line of the 5 VDC power supply. +24 VDC is the input voltage.

SAMPLE

PRINTED NAME GRADE OR TITLE AND TELEPHONE NUMBER SSG I. M. DeSpiritof 999-1776	SIGN HERE SSG I. M. DeSpiritof

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

FILL IN YOUR UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

____

____

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

POSTAGE AND FEES PAID
DEPARTMENT OF THE ARMY
DOD 314

U.S.MAIL

SAMPLE

Commander
US Army Communications-Electronics Command
and Fort Monmouth
ATTN: AMSEL-ME-MP
Fort Monmouth, New Jersey 07703-5007

TEAR ALONG PERFORATED LINE

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)

DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-6625-3041-30	7 Feb 1985	Digital Data Generator SG-1139/G

BE EXACT PIN-POINT WHERE IT IS				IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.	

PRINTED NAME GRADE OR TITLE AND TELEPHONE NUMBER	SIGN HERE

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

TEAR ALONG PERFORATED LINE

REVERSE OF DA FORM 2028-2

TEAR ALONG PERFORATED LINE

FILL IN YOUR
UNIT'S ADDRESS

FOLD BACK

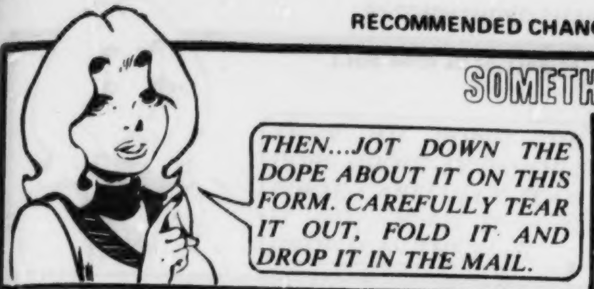
DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

POSTAGE AND FEES PAID
DEPARTMENT OF THE ARMY
DOD 314

Commander
US Army Communications-Electronics Command
and Fort Monmouth
Attn: AMSEL-ME-MP
Fort Monmouth, New Jersey 07703-5007

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS


THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

SOMETHING WRONG WITH THIS PUBLICATION?

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)

DATE SENT

PUBLICATION NUMBER TM 11-6625-3041-30	PUBLICATION DATE 7 Feb 1985	PUBLICATION TITLE Digital Data Generator SG-1139/G

BE EXACT PIN-POINT WHERE IT IS

PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.	IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:

PRINTED NAME GRADE OR TITLE AND TELEPHONE NUMBER

SIGN HERE

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

TEAR ALONG PERFORATED LINE

REVERSE OF DA FORM 2028-2

FILL IN YOUR
UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

____

____

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

POSTAGE AND FEES PAID
DEPARTMENT OF THE ARMY
DOD 314

U.S.MAIL

Commander
US Army Communications-Electronics Command
and Fort Monmouth
Attn: AMSEL-ME-MP
Fort Monmouth, New Jersey 07703-5007

RECOMMENDED CHANGES TO EQUIPMENT TECHNICAL PUBLICATIONS

SOMETHING WRONG WITH THIS PUBLICATION?

THEN...JOT DOWN THE DOPE ABOUT IT ON THIS FORM. CAREFULLY TEAR IT OUT, FOLD IT AND DROP IT IN THE MAIL.

FROM: (PRINT YOUR UNIT'S COMPLETE ADDRESS)

DATE SENT

PUBLICATION NUMBER	PUBLICATION DATE	PUBLICATION TITLE
TM 11-6625-3041-30	7 Feb 1985	Digital Data Generator SG-1139/G

BE EXACT PIN-POINT WHERE IT IS				IN THIS SPACE TELL WHAT IS WRONG AND WHAT SHOULD BE DONE ABOUT IT:
PAGE NO.	PARA-GRAPH	FIGURE NO.	TABLE NO.	

PRINTED NAME GRADE OR TITLE AND TELEPHONE NUMBER	SIGN HERE

DA FORM 1 JUL 79 2028-2

PREVIOUS EDITIONS ARE OBSOLETE

P.S.--IF YOUR OUTFIT WANTS TO KNOW ABOUT YOUR RECOMMENDATION MAKE A CARBON COPY OF THIS AND GIVE IT TO YOUR HEADQUARTERS.

TEAR ALONG PERFORATED LINE

REVERSE OF DA FORM 2028-2

FILL IN YOUR
UNIT'S ADDRESS

FOLD BACK

DEPARTMENT OF THE ARMY

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

POSTAGE AND FEES PAID
DEPARTMENT OF THE ARMY
DOD 314

Commander
US Army Communications-Electronics Command
and Fort Monmouth
Attn: AMSEL-ME-MP
Fort Monmouth, New Jersey 07703-5007

FM-913-73

CAPACITOR COLOR CODE TABLES

TABLE I - For use with Group I, Styles CM, CN, CY and CB

COLOR	MIL ID	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]				DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CY	CB	CM	CM	CM
BLACK	CM, CY CB	0	0	1			± 20 %	± 20 %		A				55 ° to + 70 °C	10 - 55 cps
BROWN		1	1	10					B	E		B			
RED		2	2	100	± 2 %		± 2 %	± 2 %	C		C			−55 ° to + 85 °C	
ORANGE		3	3	1,000		± 30 %			D				300		
YELLOW		4	4	10,000					E			D		−55 ° to + 125 °C	10 - 200 cps
GREEN		5	5		± 5 %				F				500		
BLUE		6	6											−55 ° to + 150 °C	
PURPLE (VIOLET)		7	7												
GREY		8	8												
WHITE		9	9												
GOLD				0.1			± 5 %	± 5 %							
SILVER	CN				± 10 %	± 10 %	± 10 %	± 10 %							

TABLE II - For use with Group II, General Purposes, Style CK

COLOR	TEMP. RANGE AND VOLTAGE - TEMP LIMITS[3]	Ist SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE	MIL ID
BLACK		0	0	1	± 20 %	
BROWN	AW	1	1	10	± 10 %	
RED	AX	2	2	100		
ORANGE	BX	3	3	1,000		
YELLOW	AV	4	4	10,000		CK
GREEN	CZ	5	5			
BLUE	BV	6	6			
PURPLE (VIOLET)		7	7			
GREY		8	8			
WHITE		9	9			
GOLD						
SILVER						

TABLE III - For use with Group III, Temperature Compensating, Style CC

COLOR	TEMPERATURE COEFFICIENT[4]	1st SIG FIG	2nd SIG FIG	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10uuf	CAPACITANCES 10uuf OR LESS	
BLACK	0	0	0	1		± 2.0uuf	CC
BROWN	−30	1	1	10	± 1 %		
RED	−80	2	2	100	± 2 %	± 0.25uuf	
ORANGE	−150	3	3	1,000			
YELLOW	−220	4	4				
GREEN	−330	5	5		± 5 %	± 0.5uuf	
BLUE	−470	6	6				
PURPLE (VIOLET)	−750	7	7	0.01			
GREY		8	8	0.1	± 10%		
WHITE		9	9				
GOLD	+ 100					± 1.0uuf	
SILVER							

1. The multiplier is the number by which the two significant (SIG) figures are multiplied to obtain the capacitance in uuf.

2. Letter indicate the Characteristics designated in applicable specification: MIL-C-5, MIL-C-91, MIL-C-11272, and MIL-C-10950 respectively.

3. Letters indicate the temperature range and voltage-temperature limits designated in MIL-C-11015.

4. Temperature coefficient in parts per million per degree centigrade.

EL8TH001

Figure FO-1. Color Code Marking (Sheet 1 of 3)

best copy available

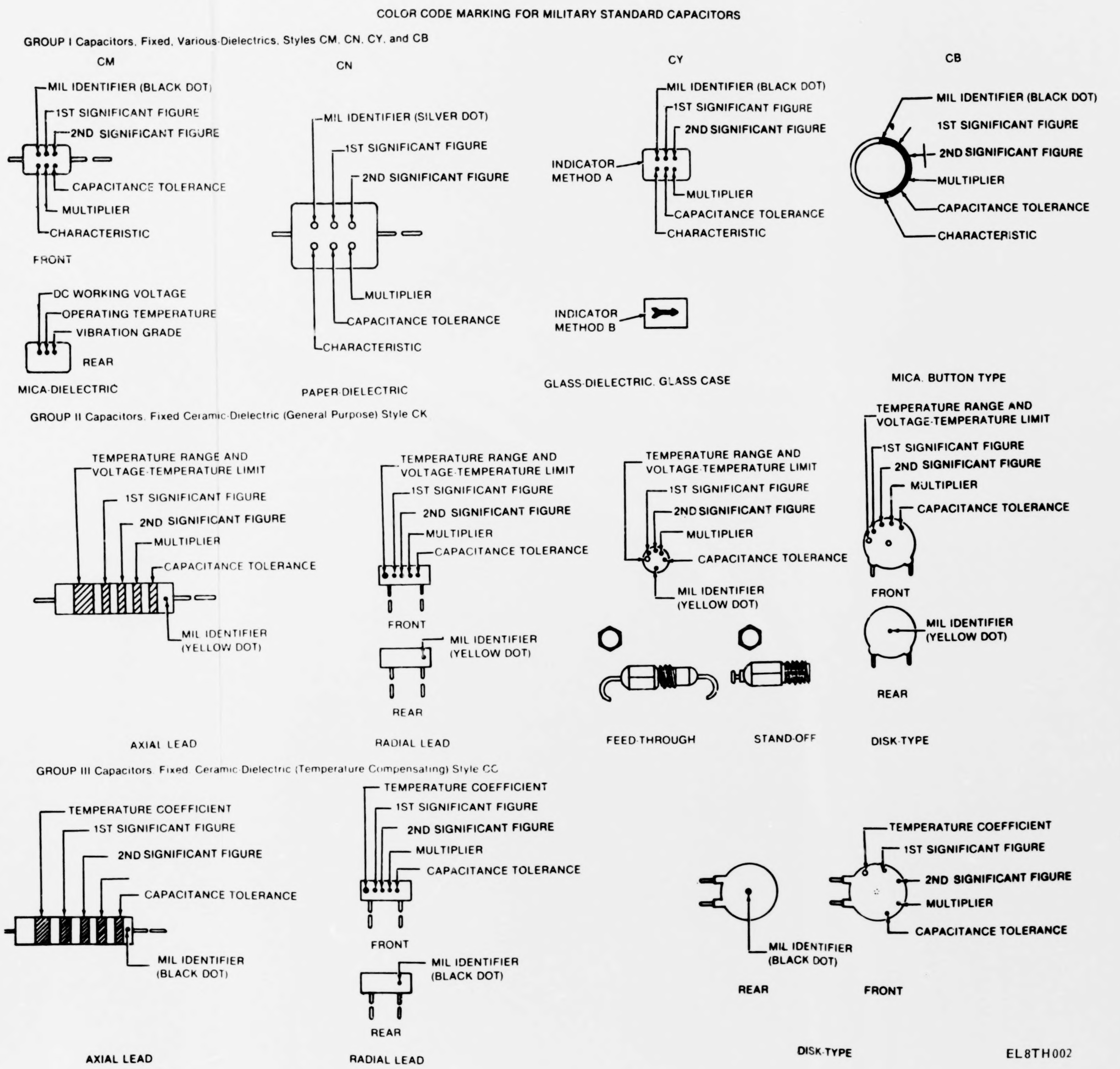


Figure FO-1. Color Code Marking (Sheet 2 of 3)

best copy available

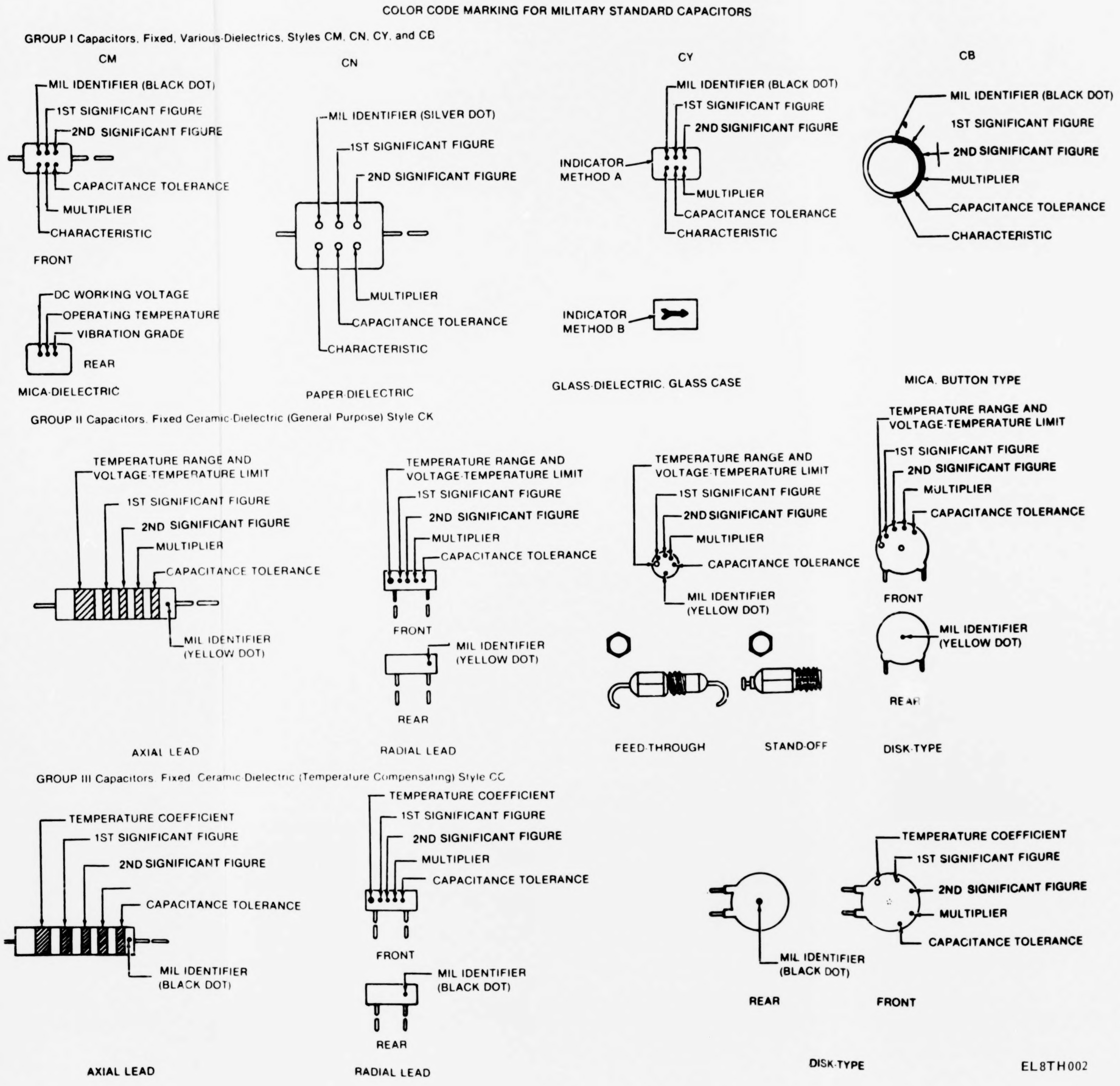
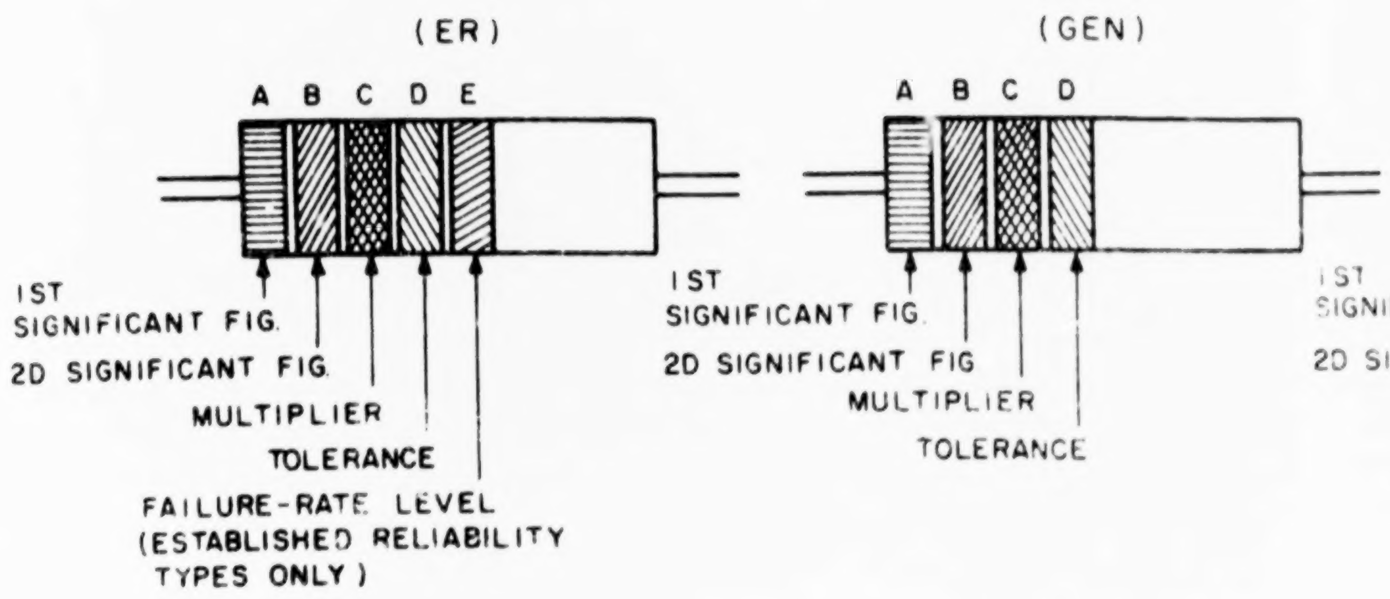
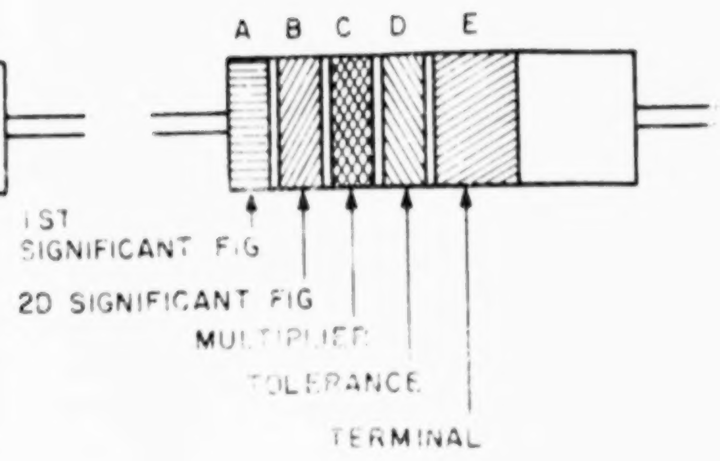


Figure FO-1. Color Code Marking (Sheet 2 of 3)

best copy available



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.



COLOR-CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE – RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS) ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS
(THESE ARE NOT COLOR CODED)

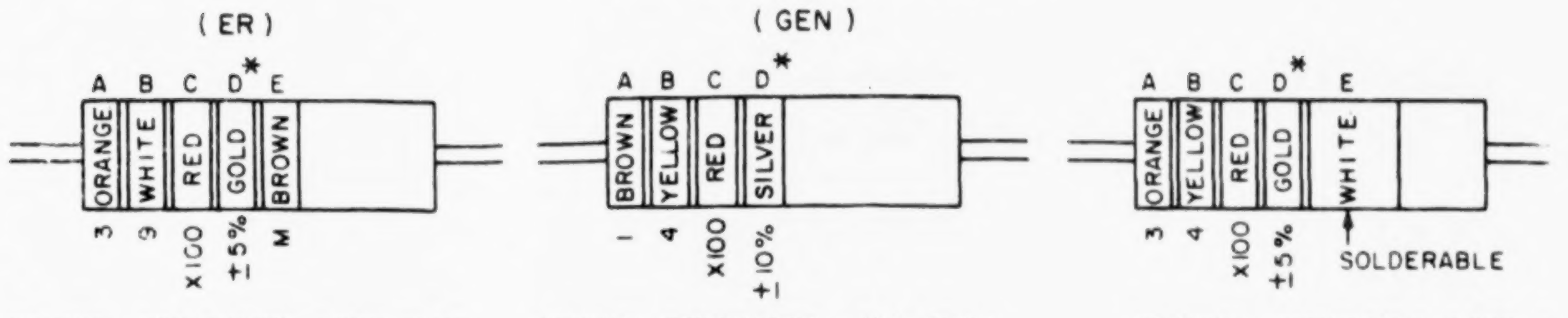
SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS   10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

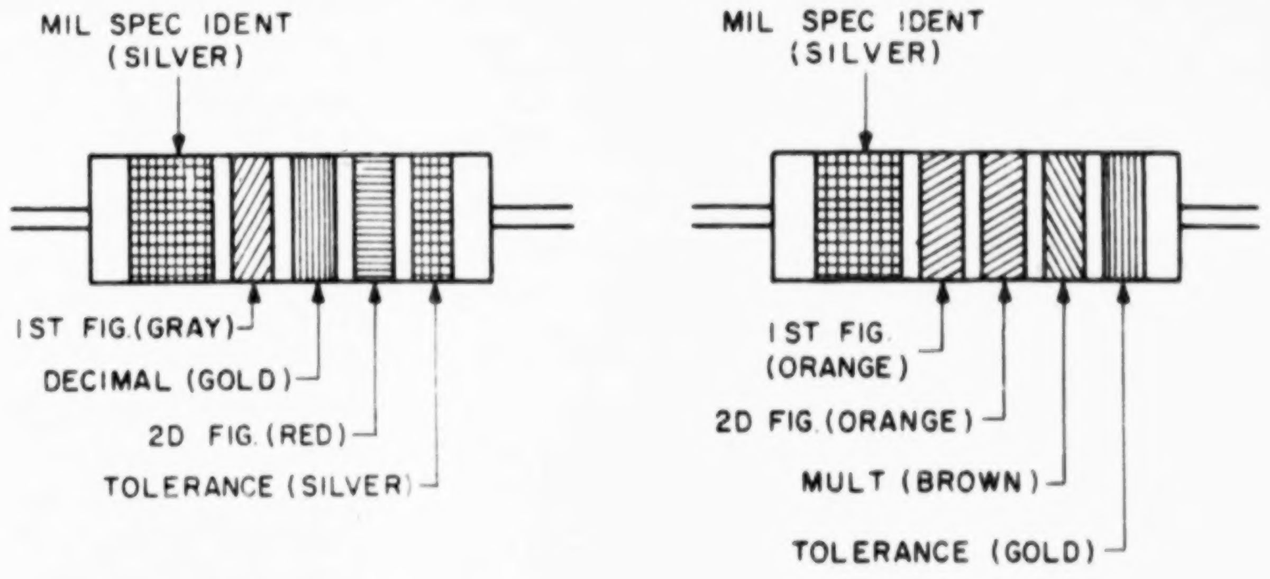
NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ± 20% AND THE RESISTOR IS NOT MIL-STD.



(A) 8.2UH ± 10%   (B) 330UH ± 5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330 UH INDUCTOR ARE ILLUSTRATED.

TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

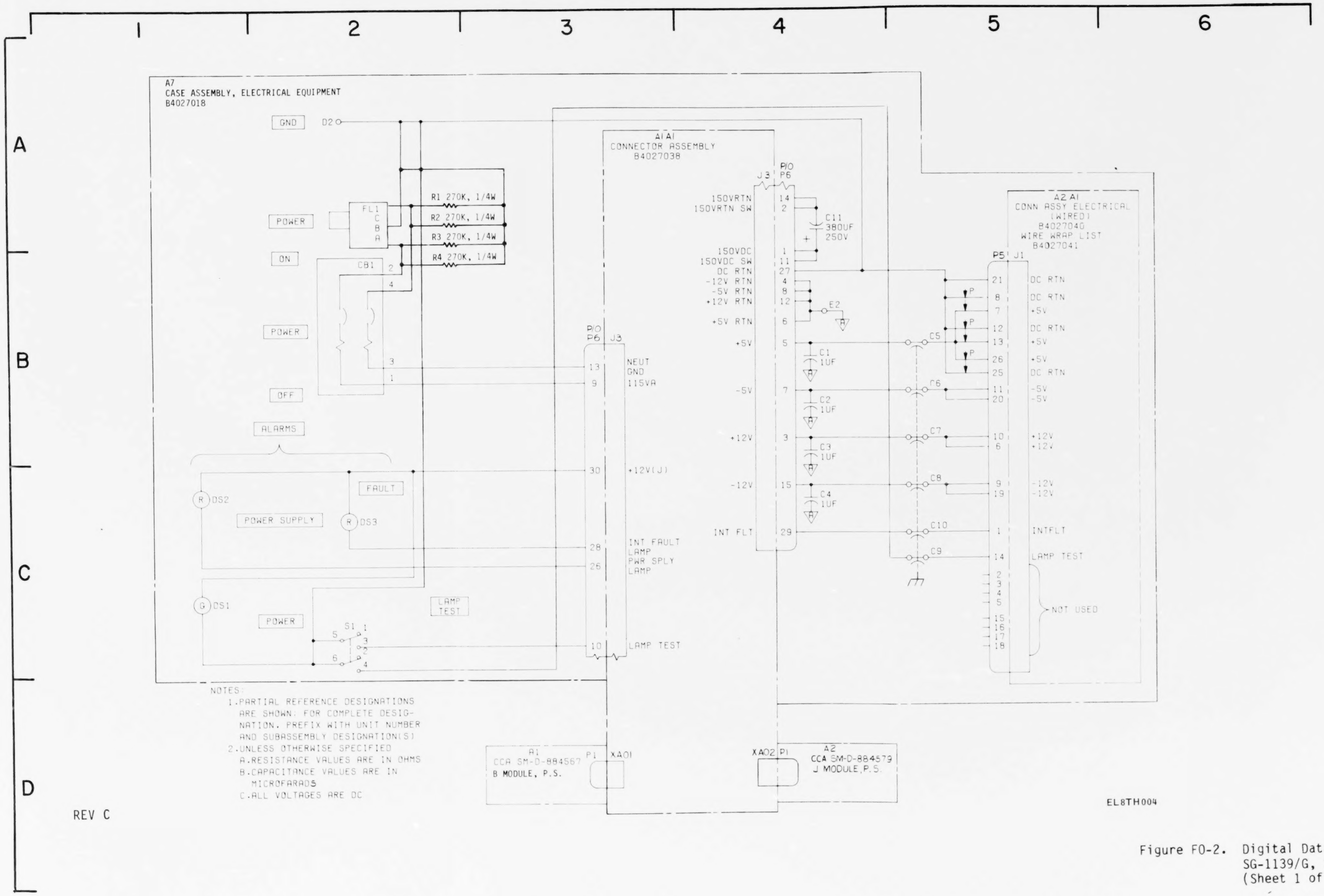
B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

FO-1 COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS AND INDUCTORS

EL8TH003

Figure FO-1. Color Code Marking
(Sheet 3 of 3)

best copy available



NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION. PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE SPECIFIED
A. RESISTANCE VALUES ARE IN OHMS
B. CAPACITANCE VALUES ARE IN MICROFARADS
C. ALL VOLTAGES ARE DC

Figure FO-2. Digital Data Generator SG-1139/G, Schematic Diagram (Sheet 1 of 3)

best copy available

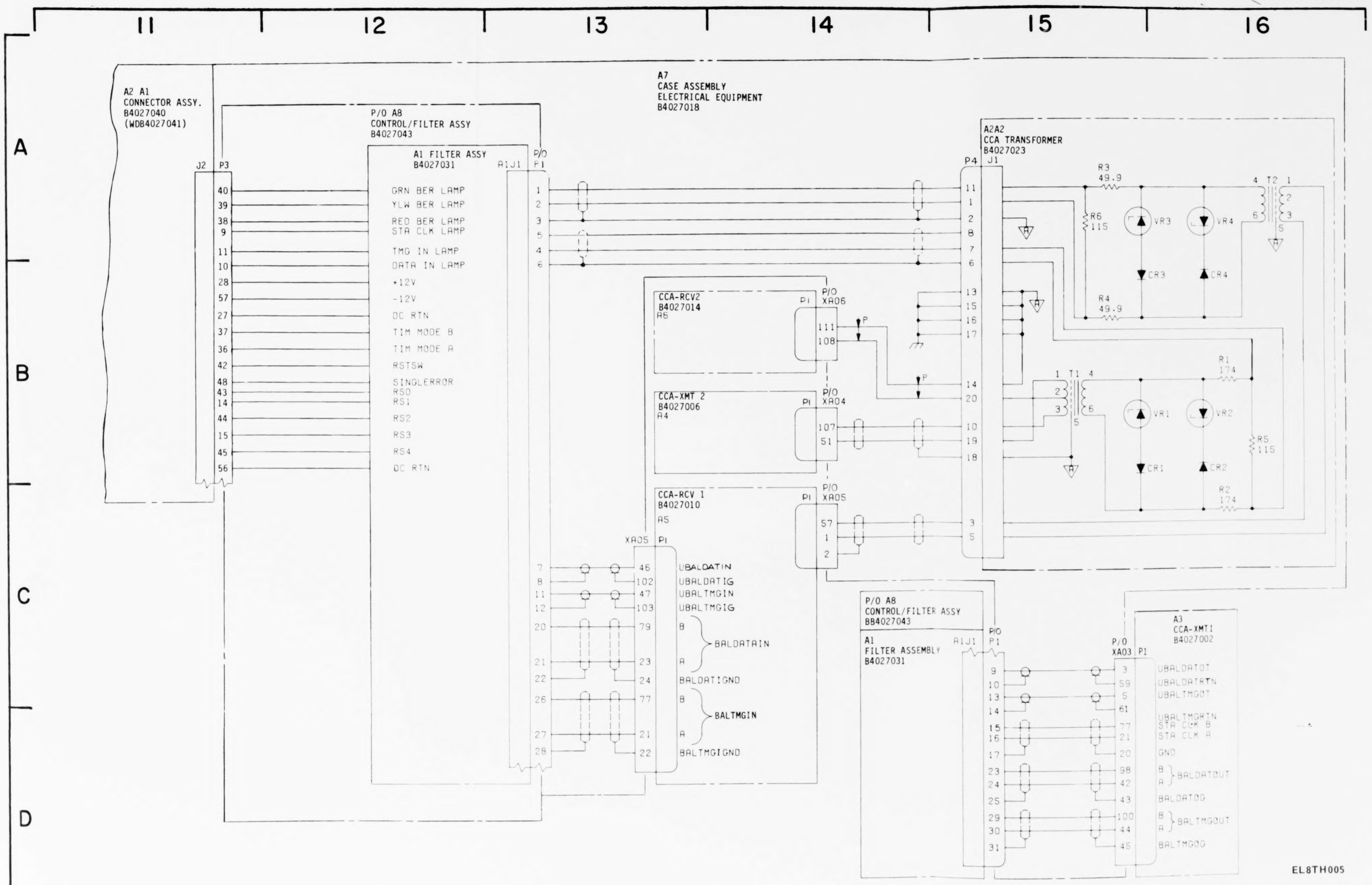


Figure FO-2. Digital Data Generator SG-1139/G, Schematic Diagram (Sheet 2 of 3)

best copy available

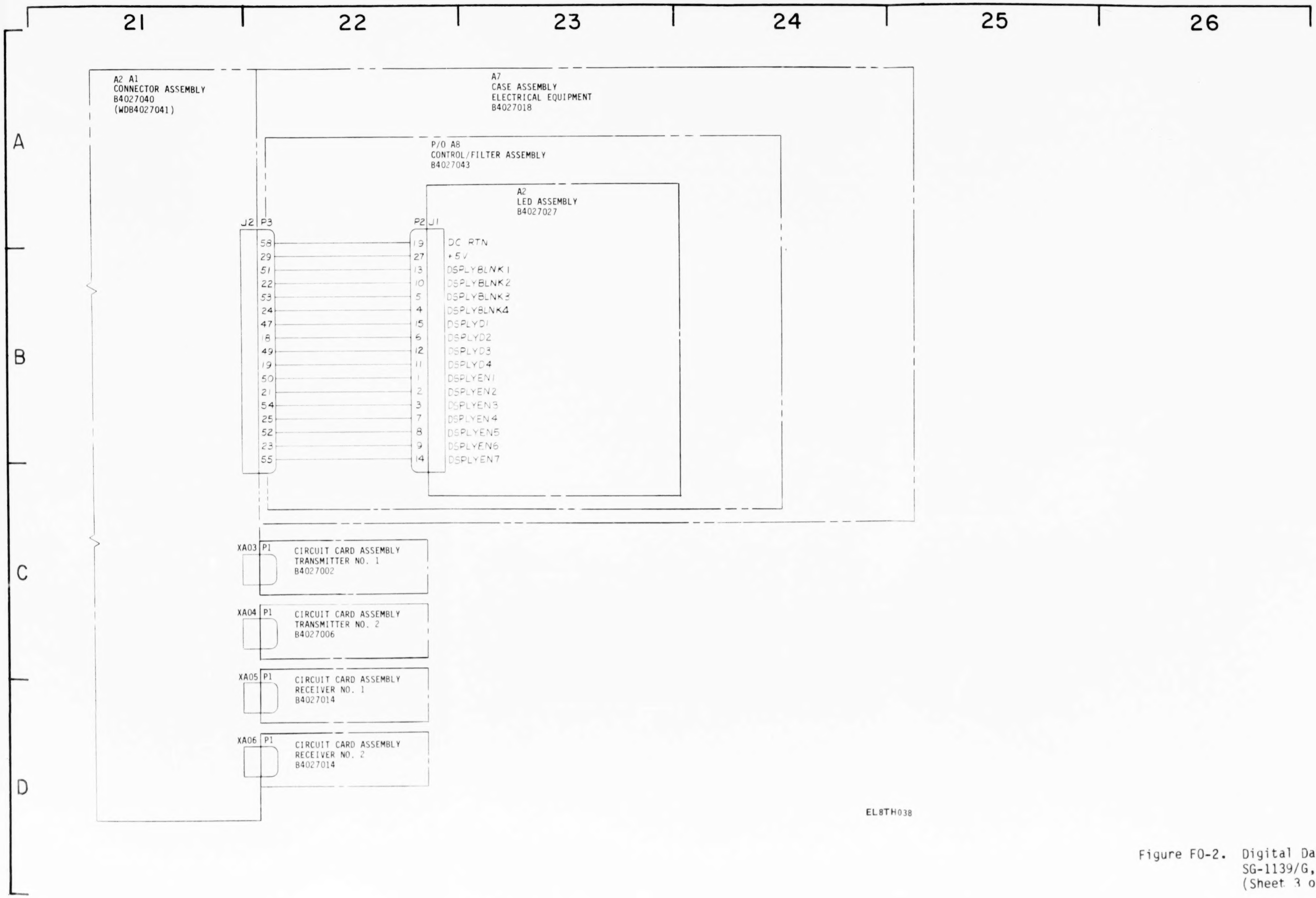
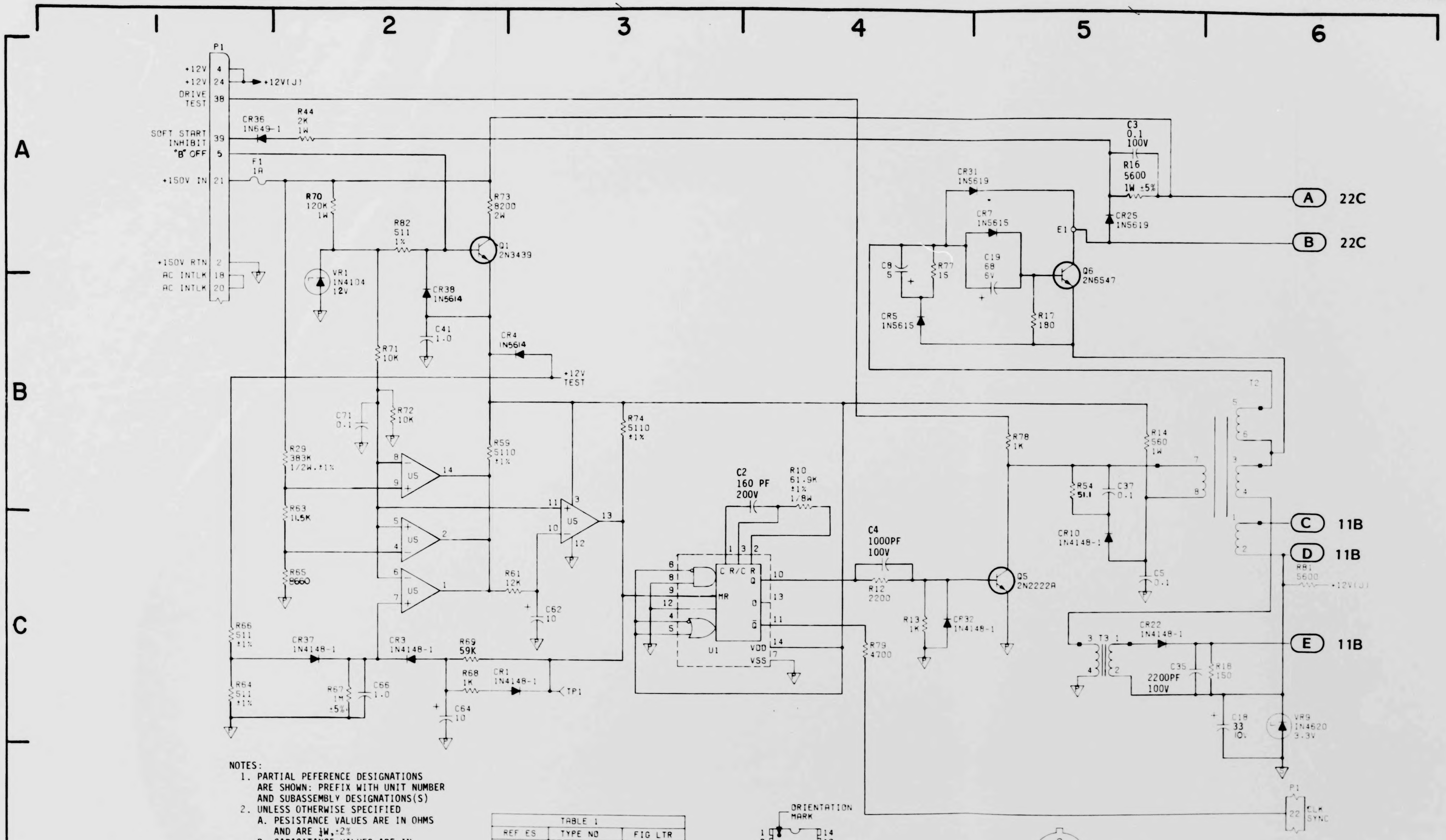


Figure FO-2. Digital Data Generator
SG-1139/G, Schematic Diagram
(Sheet 3 of 3)

best copy available



NOTES:
1. PARTIAL PEFERENCE DESIGNATIONS ARE SHOWN: PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATIONS(S)
2. UNLESS OTHERWISE SPECIFIED
   - A. PESISTANCE VALUES ARE IN OHMS AND ARE ¼W,±2%
   - B. CAPACITANCE VALUES ARE IN MICROFARADS AND ARE 50V±10%
   - C. ALL VOLTAGES ARE DC

TABLE 1

REF ES	TYPE NO	FIG LTR
U1	G166709-1	A
U2	G166712-1	A
U3	G166710-1	B
U4	G166713-1	A
U5.6.7	G166711-1	A

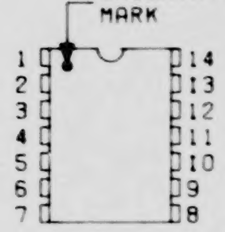


FIG A
TOP VIEW
NUMBERS ARE FOR REFERENCE ONLY

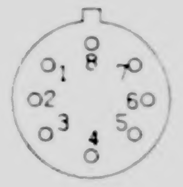


FIG B

REV F

EL8TH006

Figure FO-3. A1, Multi VDC CCA, Schematic Diagram (Sheet 1 of 4)

best copy available

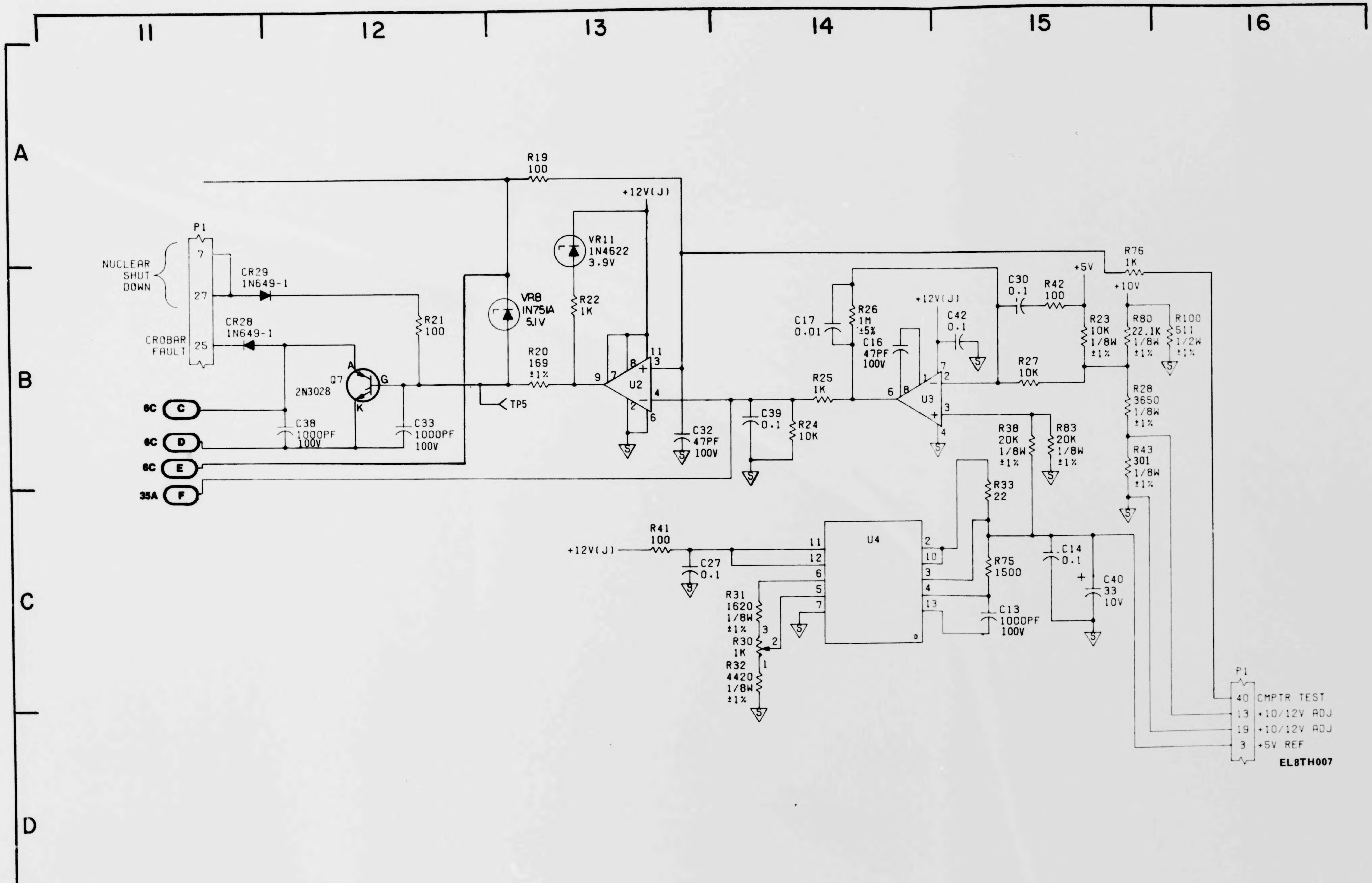


Figure FO-3. A1, Multi VDC CCA, Schematic Diagram (Sheet 2 of 4)

best copy available

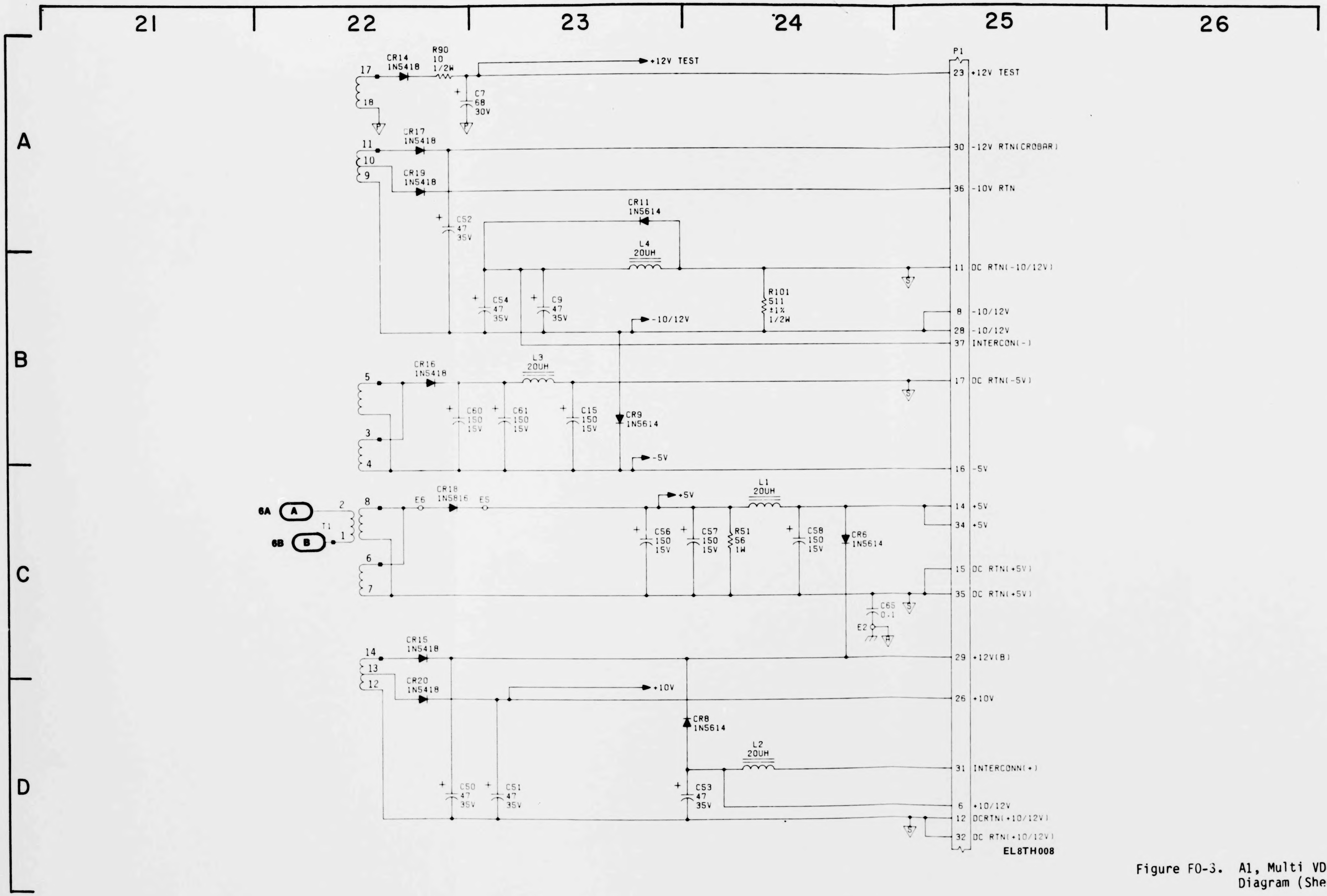


Figure FO-3. A1, Multi VDC CCA, Schematic Diagram (Sheet 3 of 4)

best copy available

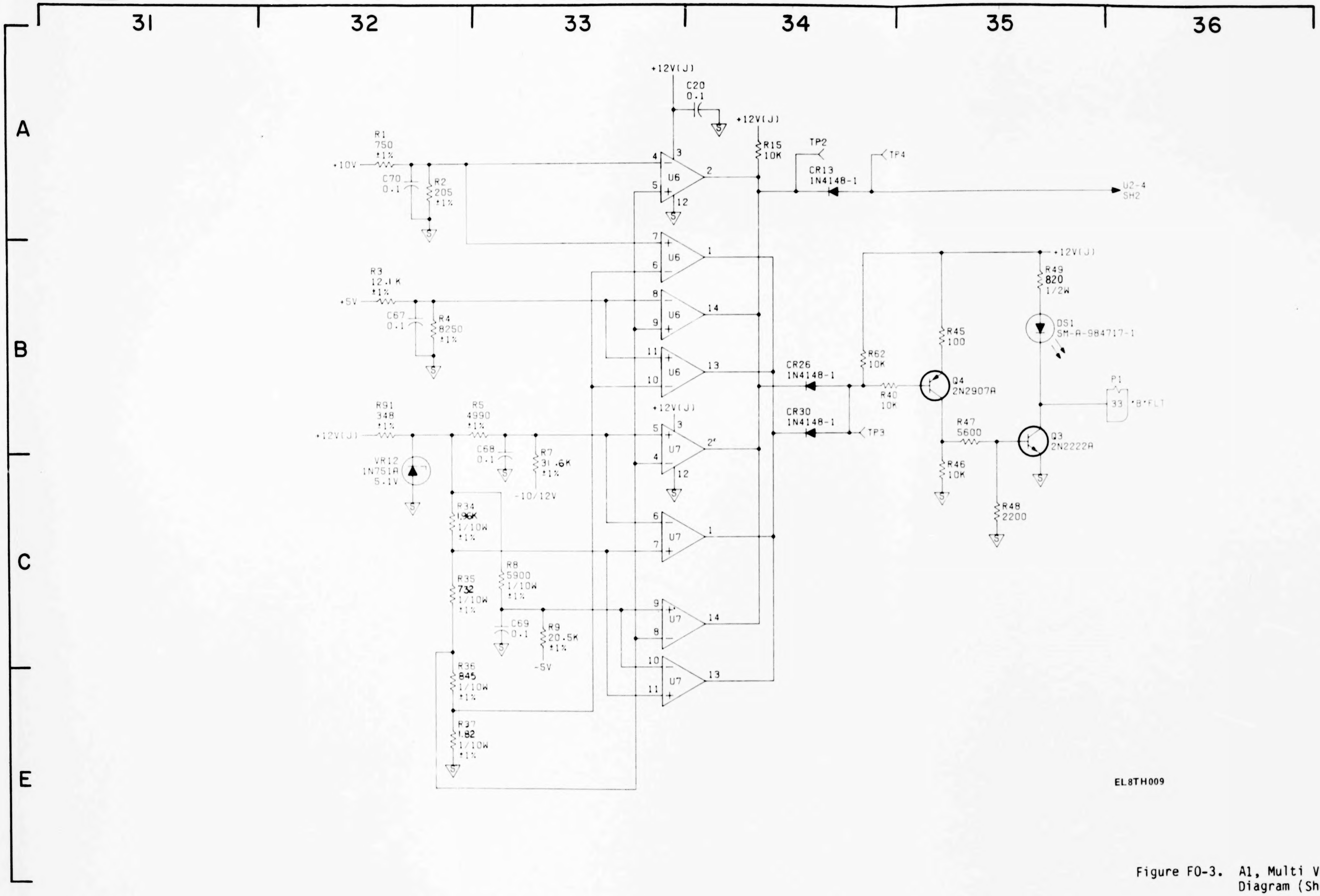
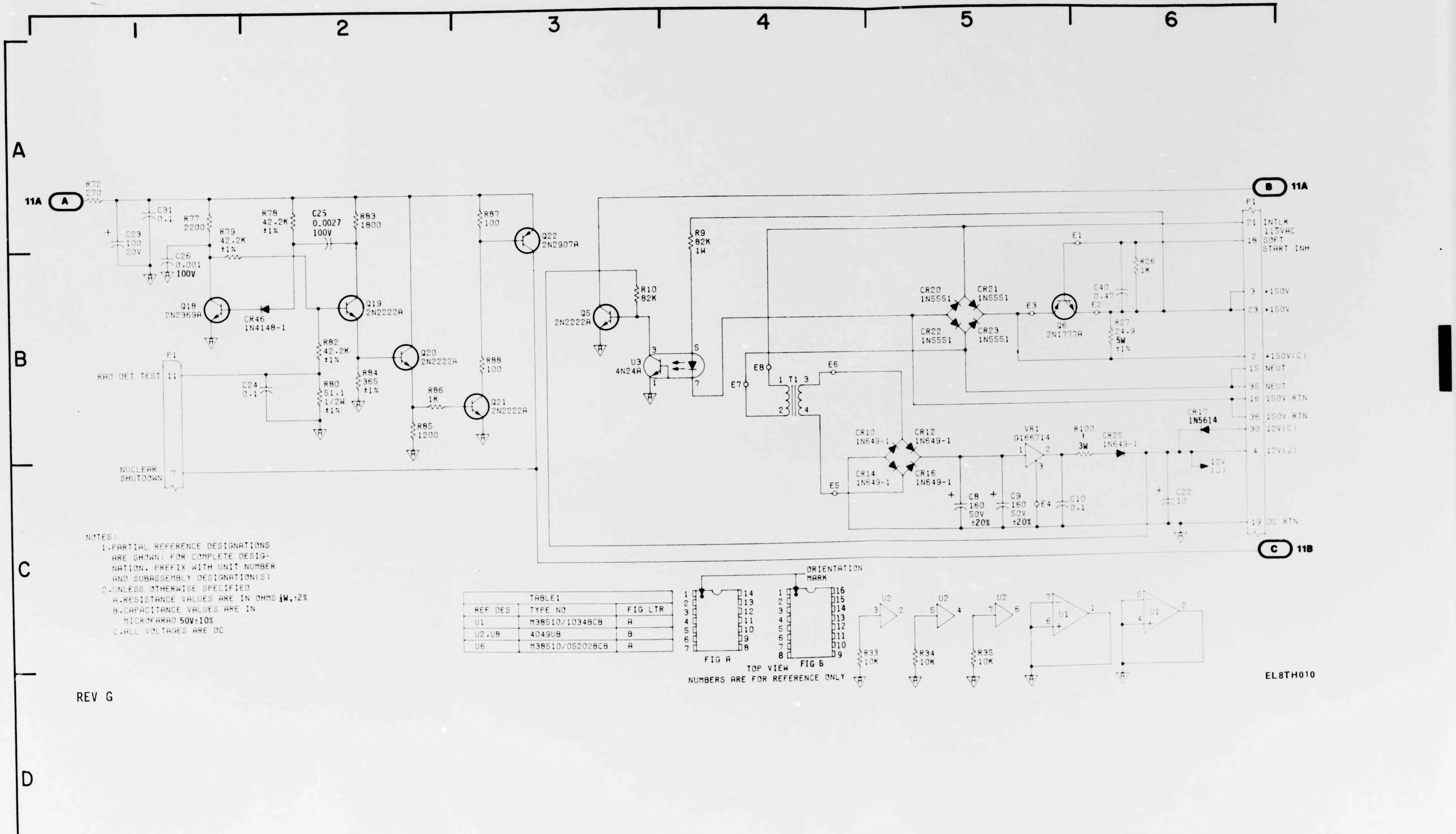


Figure FO-3. A1, Multi VDC CCA, Schematic Diagram (Sheet 4 of 4)

best copy available



NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION. PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE SPECIFIED
A. RESISTANCE VALUES ARE IN OHMS ¼W, ±2%
B. CAPACITANCE VALUES ARE IN MICROFARAD 50V±10%
C. ALL VOLTAGES ARE DC

TABLE1

REF DES	TYPE NO	FIG LTR
U1	M38510/10348CB	A
U2.U8	4049UB	B
U6	M38510/05202BCB	A

REV G

Figure FO-4. A2, AC Input CCA, Schematic Diagram (Sheet 1 of 2)

best copy available

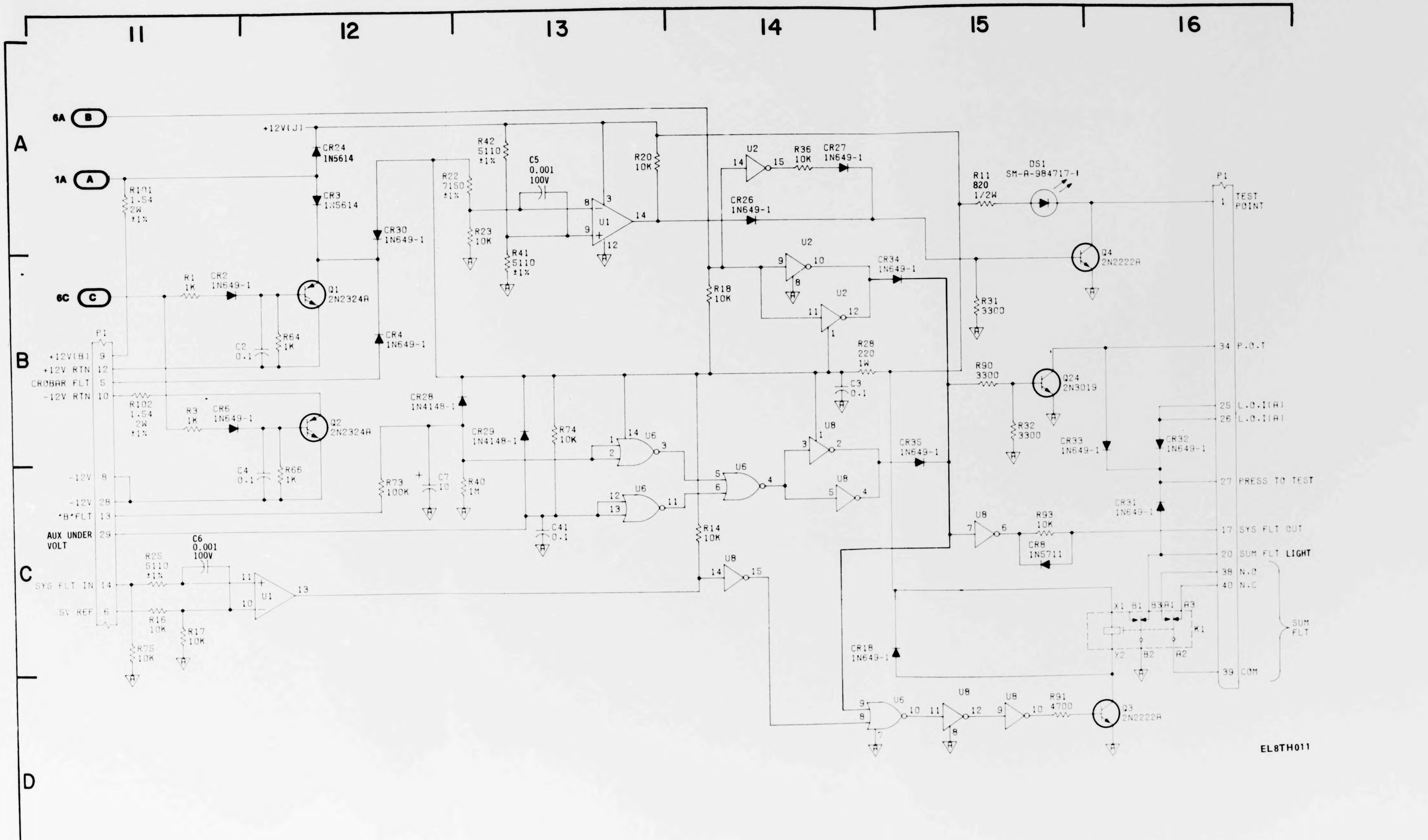


Figure FO-4. A2, AC Input CCA, Schematic Diagram (Sheet 2 of 2)

best copy available

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE SPECIFIED:
   - A. RESISTOR VALUES ARE IN OHMS AND ARE 1/4W, ±20%
   - B. CAPACITANCE VALUES ARE IN MICROFARADS AND ARE 50V, ±10%
   - C. ALL VOLTAGES ARE DC
3. ☐ INDICATES MARKING

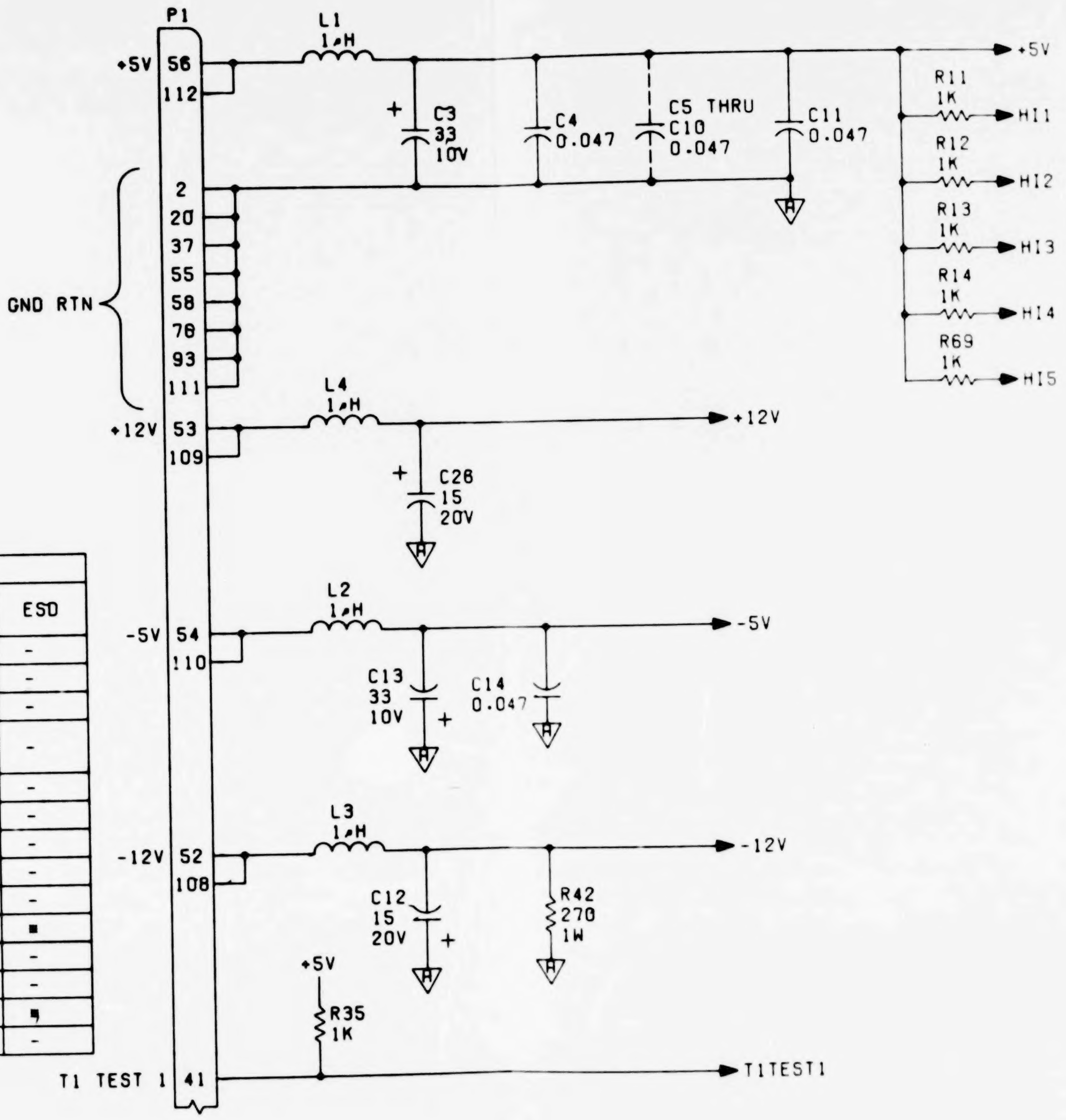


TABLE 1

REF DES	TYPE	PWR PINS +5V	PWR PINS -5V	PWR PINS GND	FIG LTR	ESD
U3.6.23.31	M38510/30001BCX	14	-	7	A	-
U13.19.36	M38510/30003BCX	14	-	7	A	-
U12.21	M38510/30302BCX	14	-	7	A	-
U2.5.8.9.14.18.20.24.25.29.30	M38510/30102BCX	14	-	7	A	-
U16	M38510/30502BCX	14	-	7	A	-
U15	M38510/30901BEX	16	-	8	B	-
U4.27	M38510/30902BEX	16	-	8	B	-
U7.10.11	M38510/31504BEX	16	-	8	B	-
U17.22	M38510/30605BCX	14	-	7	A	-
U34	M38510/20702BEX	16	-	8	B	■
U26.32.35	M38510/10401BCX	14	13	7	A	-
U28	54F74	14	-	7	A	-
U1	M38510/05503BEX	16	-	8	A	■
U33	SM-A-876228	14	11	7	A	-

TABLE 2

REF DES

HIGHEST USED	NOT USED
C29	
CR5	
DS1	
L5	
P1	
Q7	
R71	
U36	
VR1	
Y1	

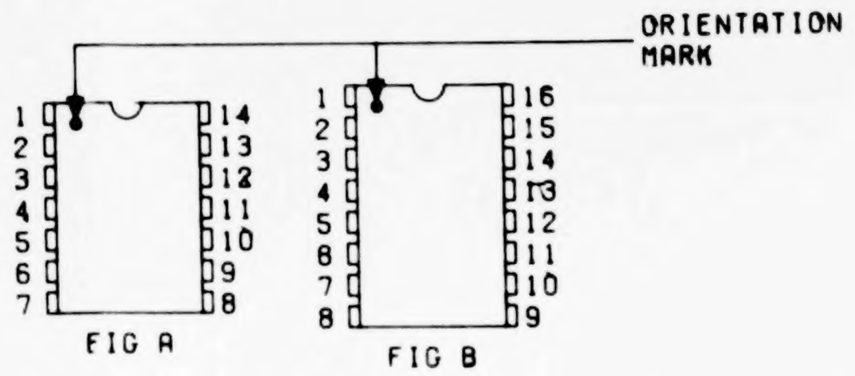
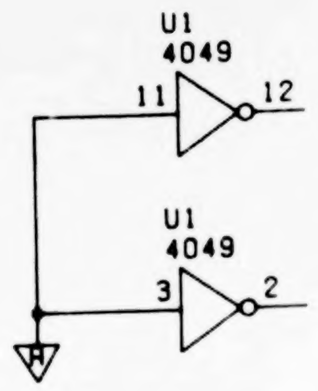


FIG A FIG B

TOP VIEW
NUMBERS ARE FOR REFERENCE ONLY



NOT USED

REV L

EL8TH012

Figure FO-5. A3, Transmit 1 CCA, Schematic Diagram (Sheet 1 of 6)

best copy available

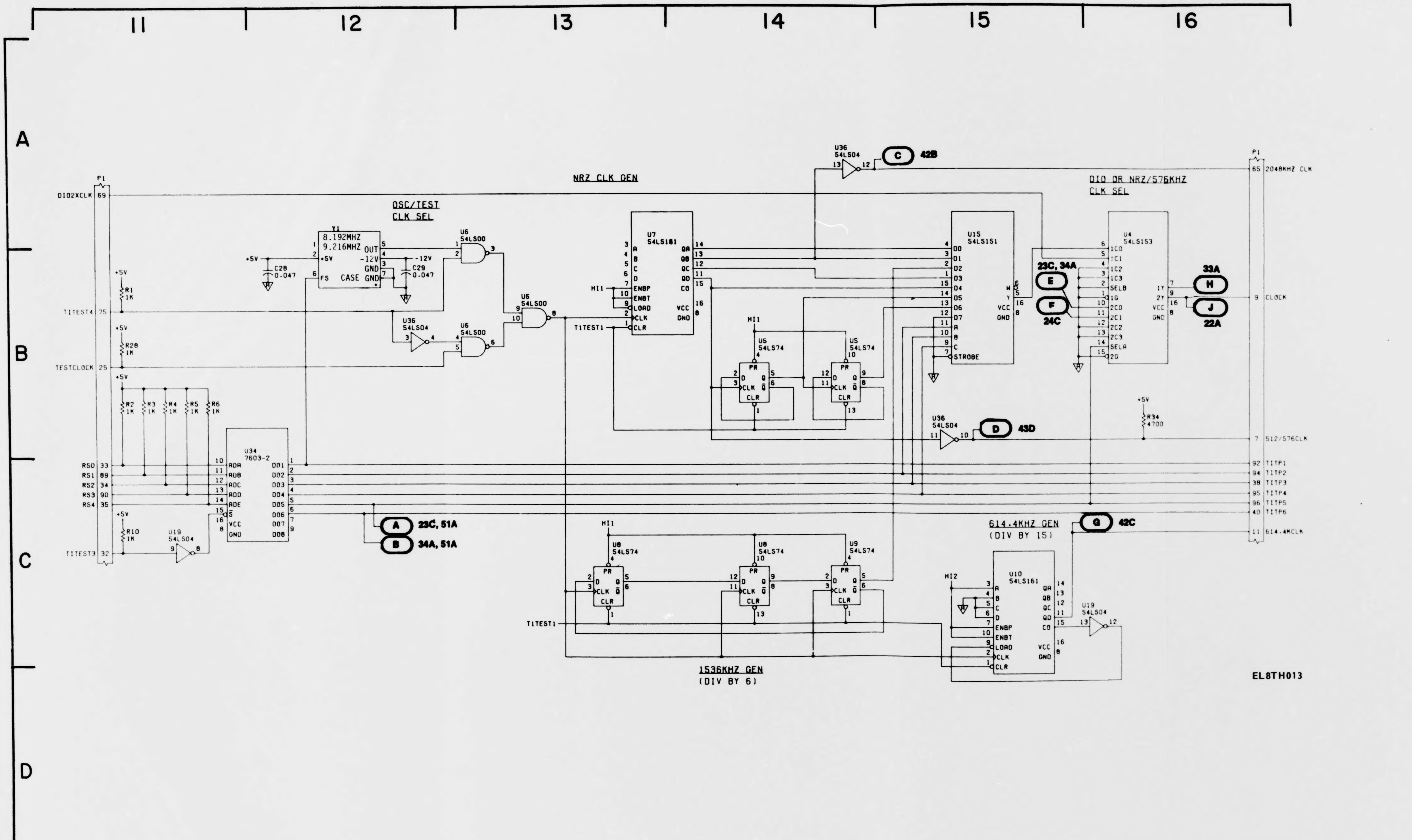


Figure FO-5. A3, Transmit 1 CCA, Schematic Diagram (Sheet 2 of 6)

best copy available

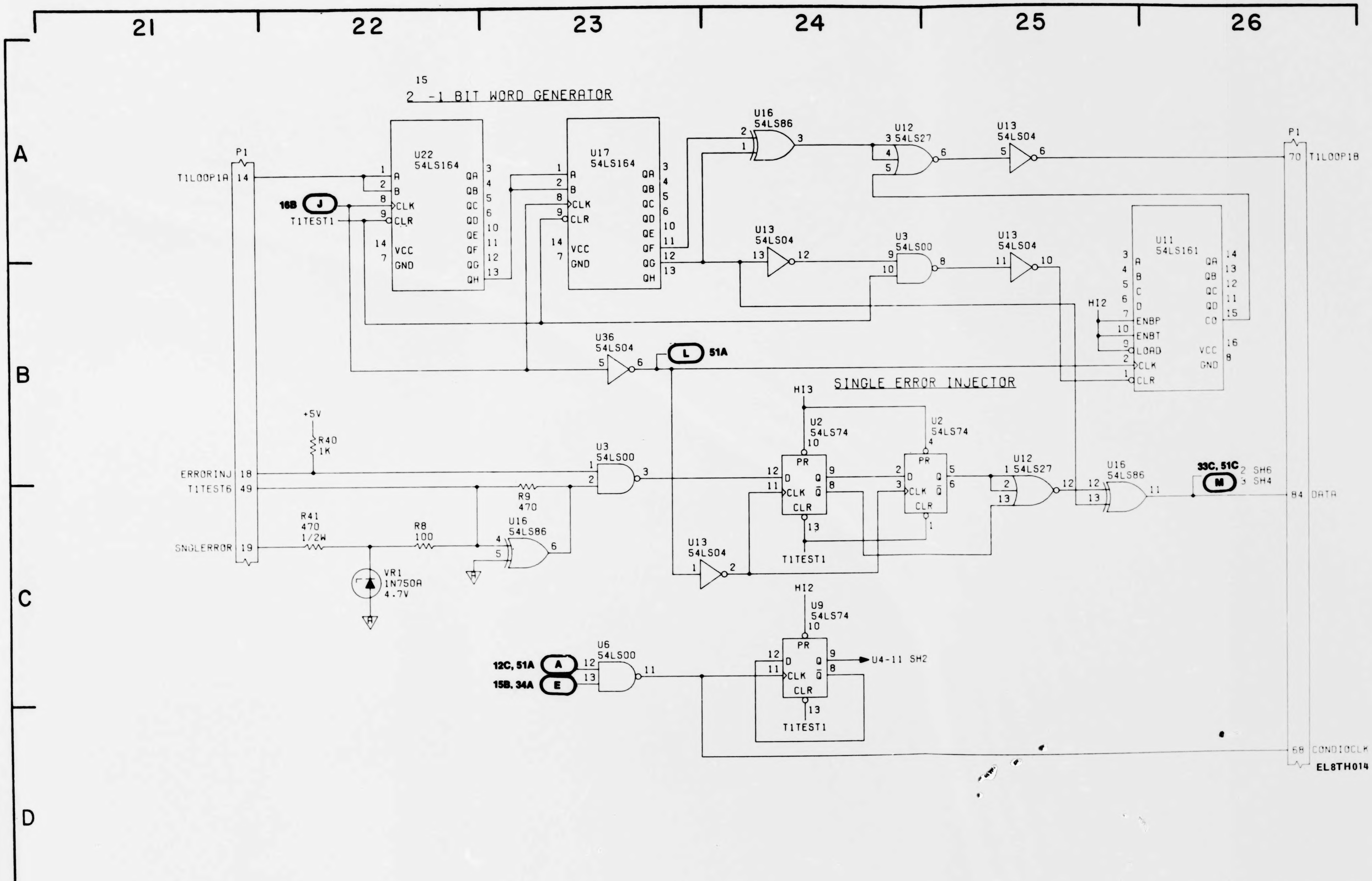


Figure FO-5. A3, Transmit 1 CCA, Schematic Diagram (Sheet 3 of 6)

best copy available

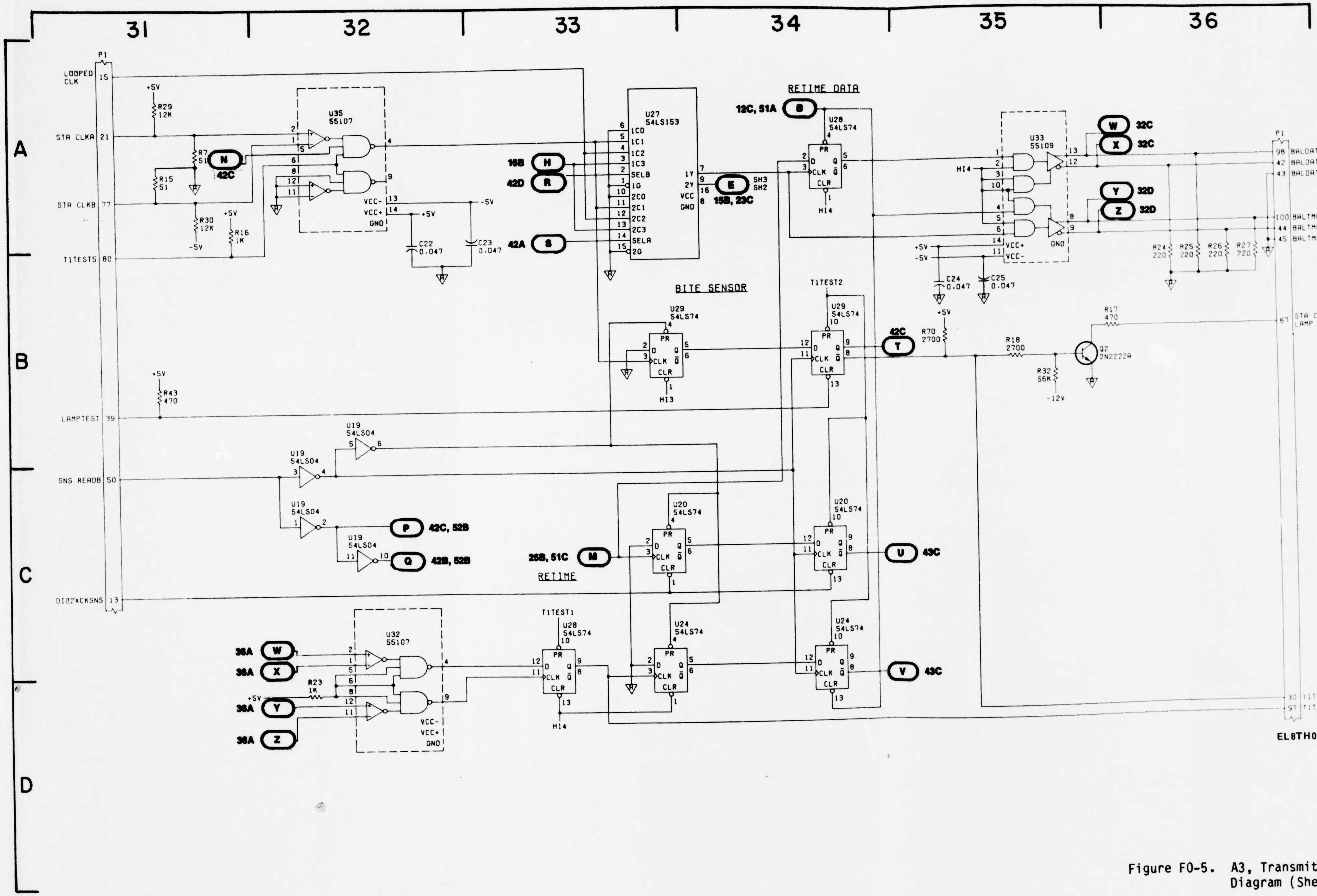


Figure FO-5. A3, Transmit 1 CCA, Schematic Diagram (Sheet 4 of 6)

best copy available

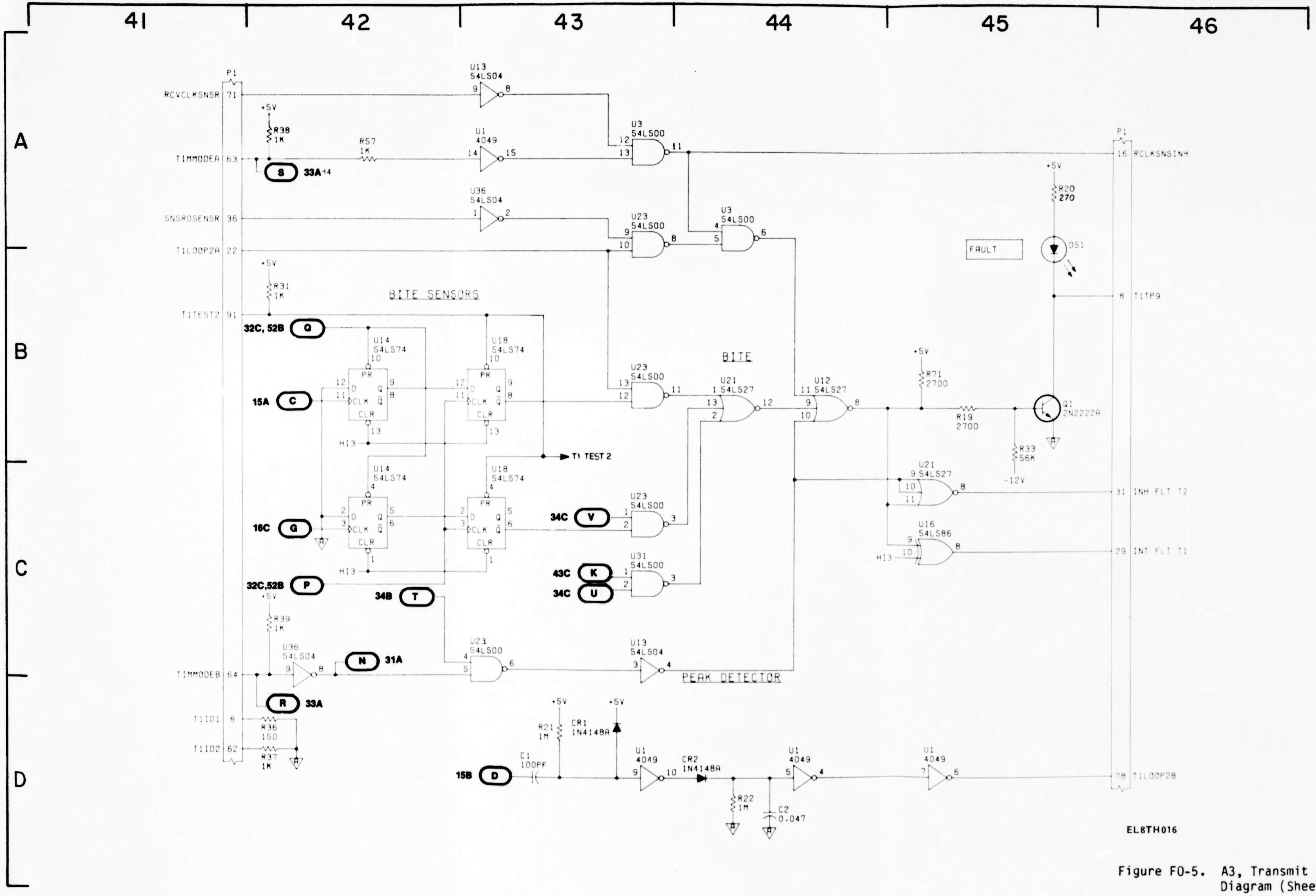


Figure FO-5. A3, Transmit 1 CCA, Schematic Diagram (Sheet 5 of 6)

best copy available

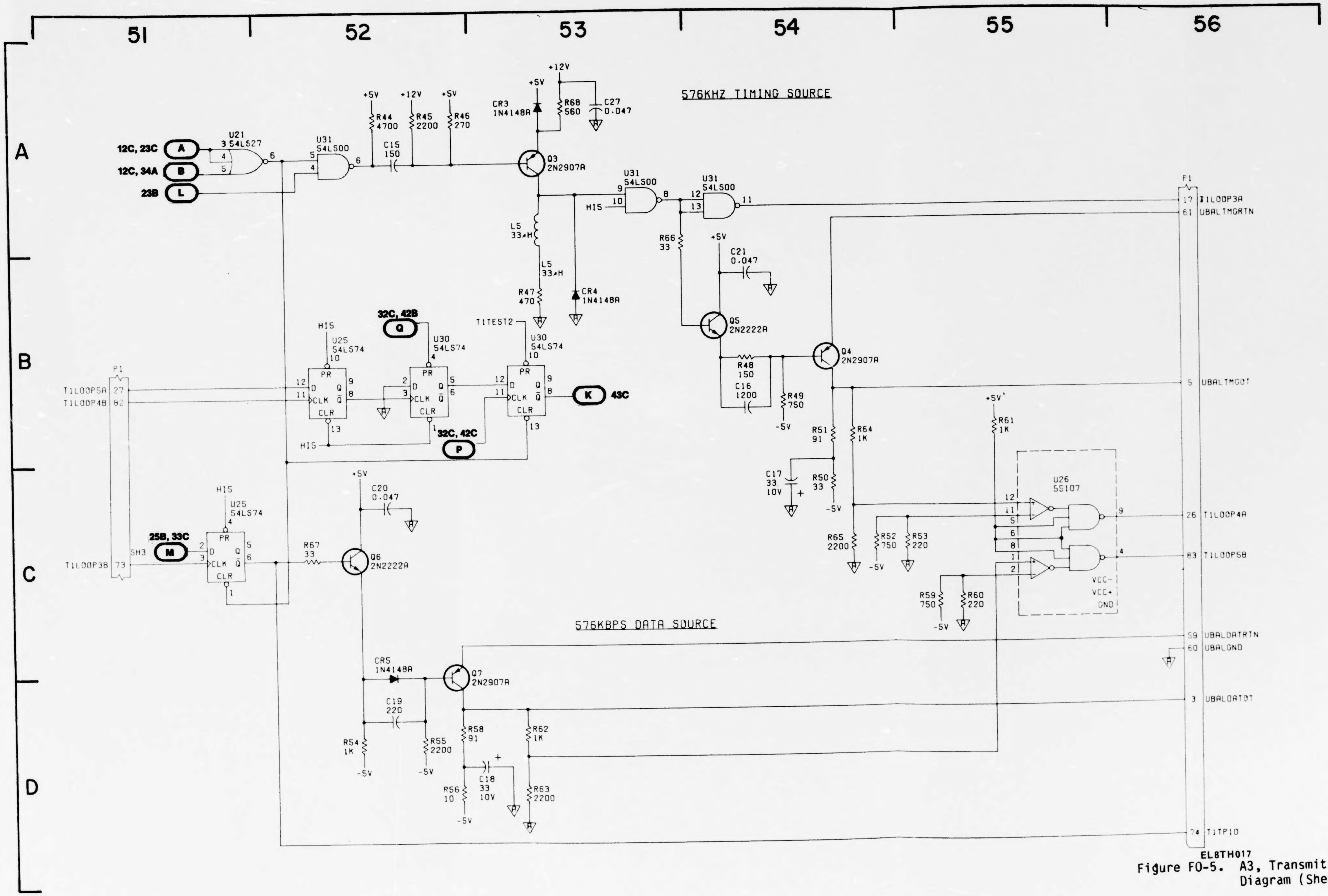


Figure FO-5. A3, Transmit 1 CCA, Schematic Diagram (Sheet 6 of 6)

best copy available

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:FOR COMPLETE DESIGNATION.PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE SPECIFIED
   A. RESISTOR VALUES ARE IN OHMS AND ARE 1/4W.2%
   B. CAPACITANCE VALUES ARE IN MICROFARADS AND ARE 50V.±10%
   C. ALL VOLTAGES ARE DC
3. ☐ INDICATES MARKING

TABLE 1

REF DES	TYPE	PWR PINS +5V	-5V	GND	FIG LTR	ESD
U1.3.12.35	M38510/30001BCX	14	-	7	A	-
U10.28.42	M38510/30003BCX	14	-	7	A	-
U36	M38510/30302BCX	14	-	7	A	-
U13.14.40	M38510/30203BCX	14	-	7	A	-
U2.5.8.9.18.19.34.41	M38510/30102BCX	14	-	7	A	-
U37	M38510/30701BEX	16	-	8	B	-
U7.16.24.30.32	M38510/30901BEX	16	-	8	B	-
U6.15.17.23.25.29.31	M38510/31503BEX	16	-	8	B	-
U4.11.20.21.22.26.33	M38510/31504BEX	16	-	8	B	-
U39	M38510/20702BEX	16	-	8	B	-
U38	M38510/10401BCX	14	13	7	A	-
U27	M38510/05503BEX	1	-	8	B	■

TABLE 2

REF DES HIGHEST USED	NOT USED
C19	
CR2	
DS1	
L4	
P1	
Q3	
R65	R13-16.20.21.25.28-38.40-43.56.57
U42	

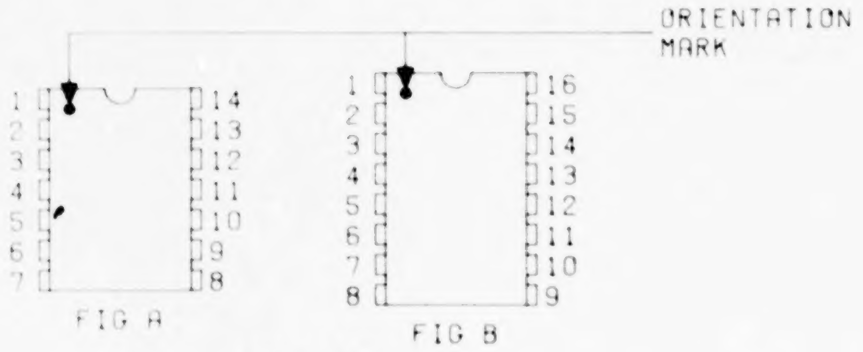
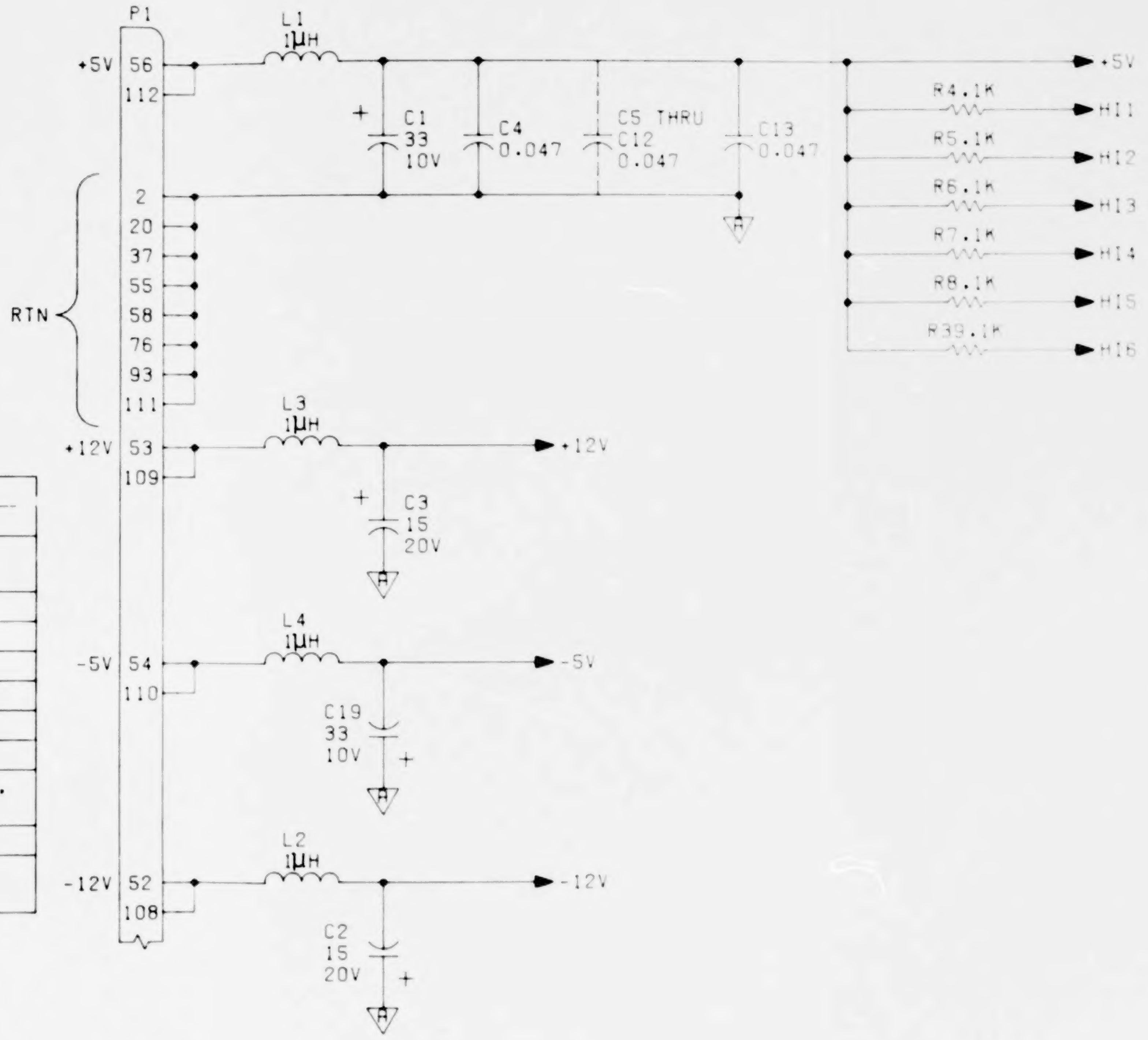
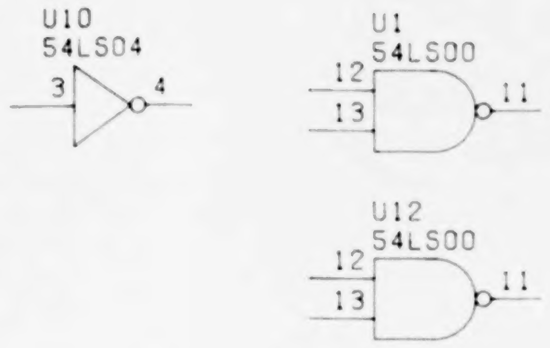


FIG A FIG B

TOP VIEW
NUMBERS ARE FOR REFERENCE ONLY





NOT USED

REV H

EL8TH018

Figure FO-6. A4, Transmit 2 CCA, Schematic Diagram (Sheet 1 of 6)

best copy available

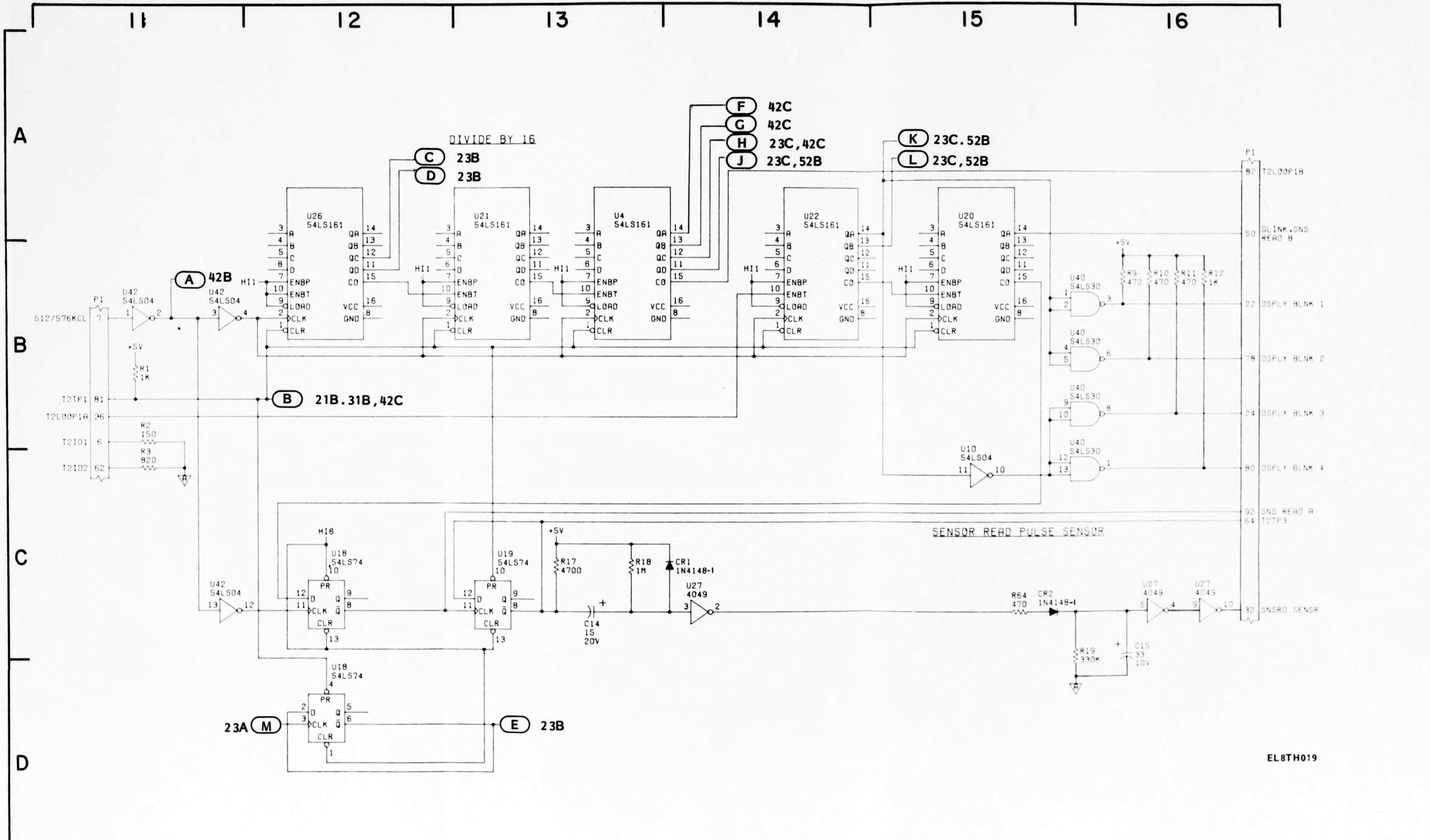


Figure FO-6. A4, Transmit 2 CCA, Schematic Diagram (Sheet 2 of 6)

best copy available

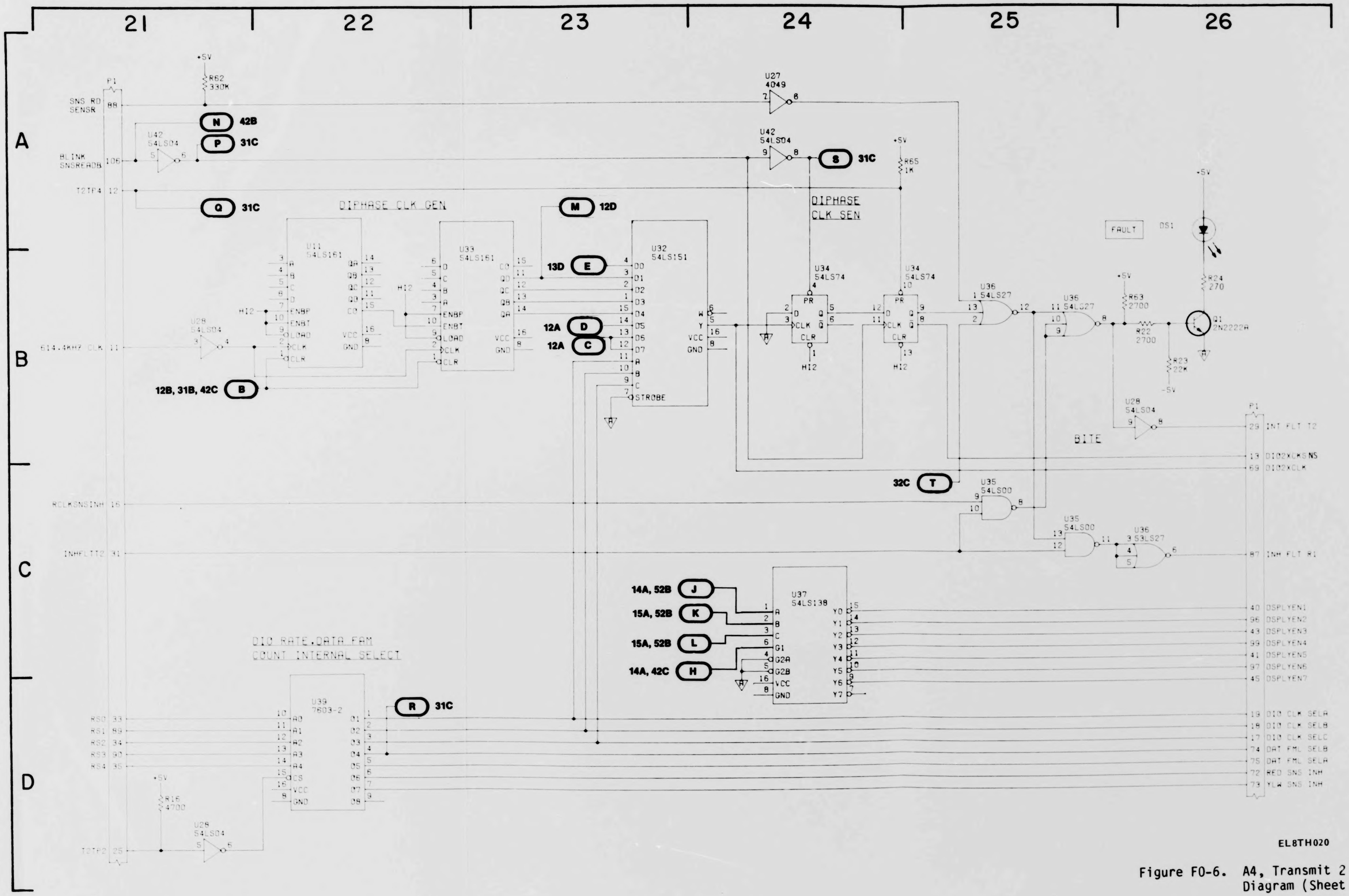


Figure FO-6. A4, Transmit 2 CCA, Schematic Diagram (Sheet 3 of 6)

best copy available

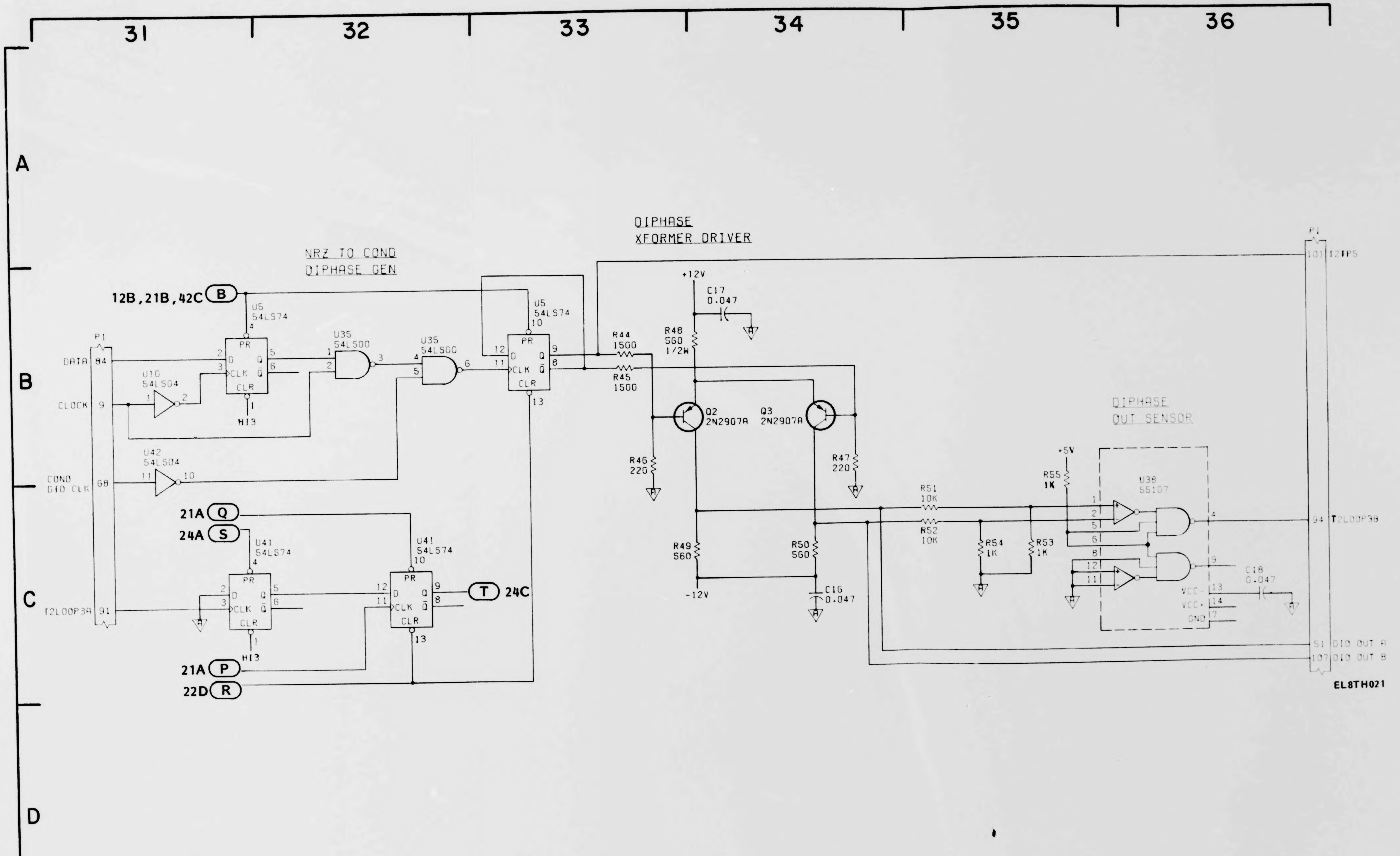
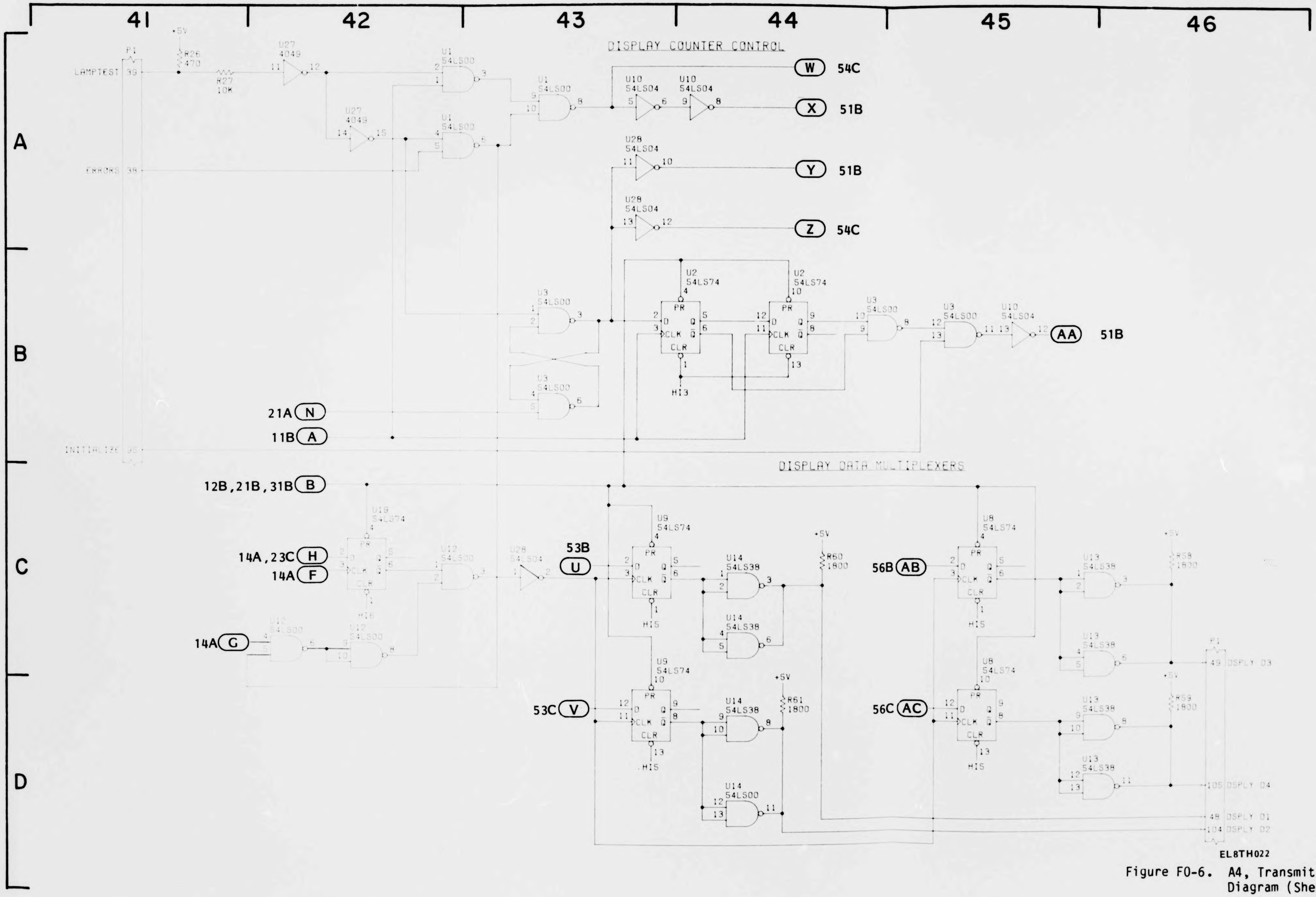


Figure FO-6. A4, Transmit 2 CCA, Schematic Diagram (Sheet 4 of 6)

best copy available



EL8TH022

Figure FO-6. A4, Transmit 2 CCA, Schematic Diagram (Sheet 5 of 6)

best copy available

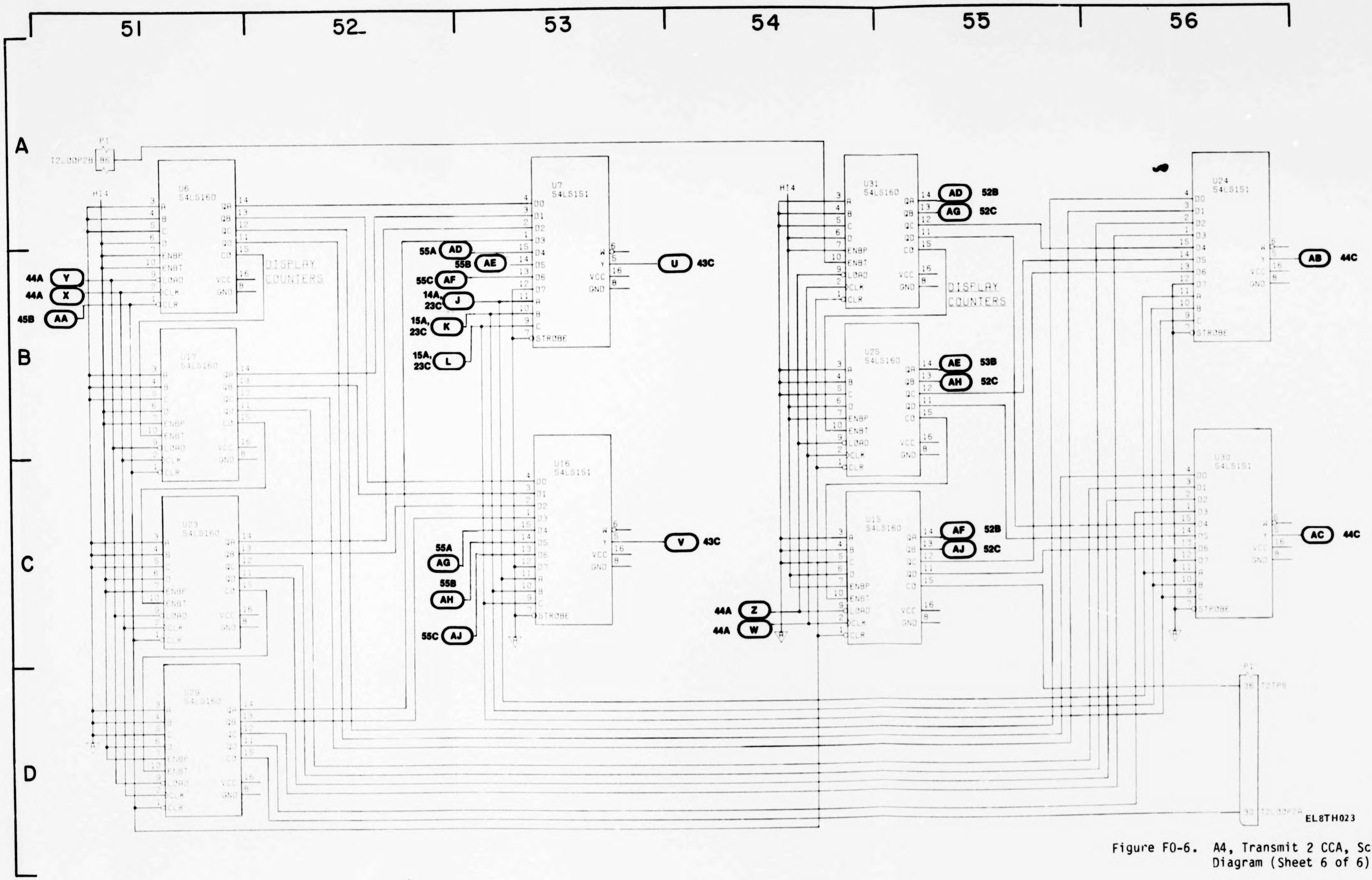


Figure FO-6. A4, Transmit 2 CCA, Schematic Diagram (Sheet 6 of 6)

best copy available

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE SPECIFIED:
   A. RESISTOR VALUES ARE IN OHMS AND ARE 1/4W, ±2%
   B. CAPACITOR VALUES ARE IN MICROFARADS AND ARE 50V, ±10%
   C. ALL VOLTAGES ARE DC
3. ☐ INDICATES FRONT PANEL MARKING

TABLE 1

REF DES	TYPE	POWER PINS					FIG LTR	ESD
		+5V	-5V	+12V	-12V	GND		
U3.17.30.34	M38510/30001BCX	14	-	-		7	A	-
U19.29	M38510/30003BCX	14	-	-		7	A	-
U12.20	M38510/30302BCX	14	-	-		7	A	-
U1.2.4.5.8. 13-15.18.23-25 U27.28.31.38	M38510/30102BCX	14	-	-	-	7	A	-
U33.35	M38510/30502BCX	14	-	-		7	A	-
U22.37	M38510/30901BEX	16	-	-		8	B	-
U7	M38510/30902BEX	16	-	-		8	B	-
U10.11.21	M38510/31504BEX	16	-	-		8	B	-
U9.16.26	M38510/30605BCX	14	-	-		7	A	-
U32.36	M38510/10401BCX	14	13	-		7	A	-
U39	M38510/10305BEX	-	-	1.9	5	-	B	-
U6	M38510/05503BEX	1	-	-		8	B	■

TABLE 2

REF DES	
HIGHEST USED	NOT USED
C26	
DS1	
L4	
P1	
Q5	
R52	R22.31
U39	

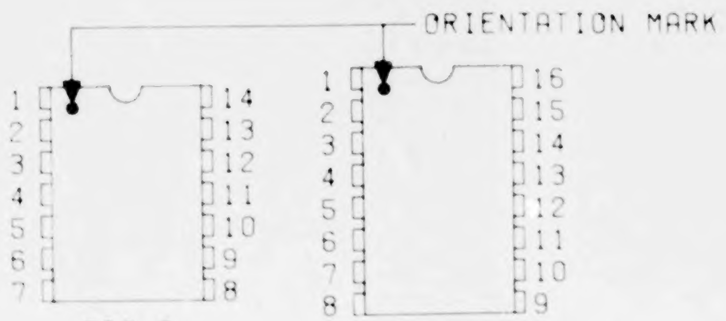
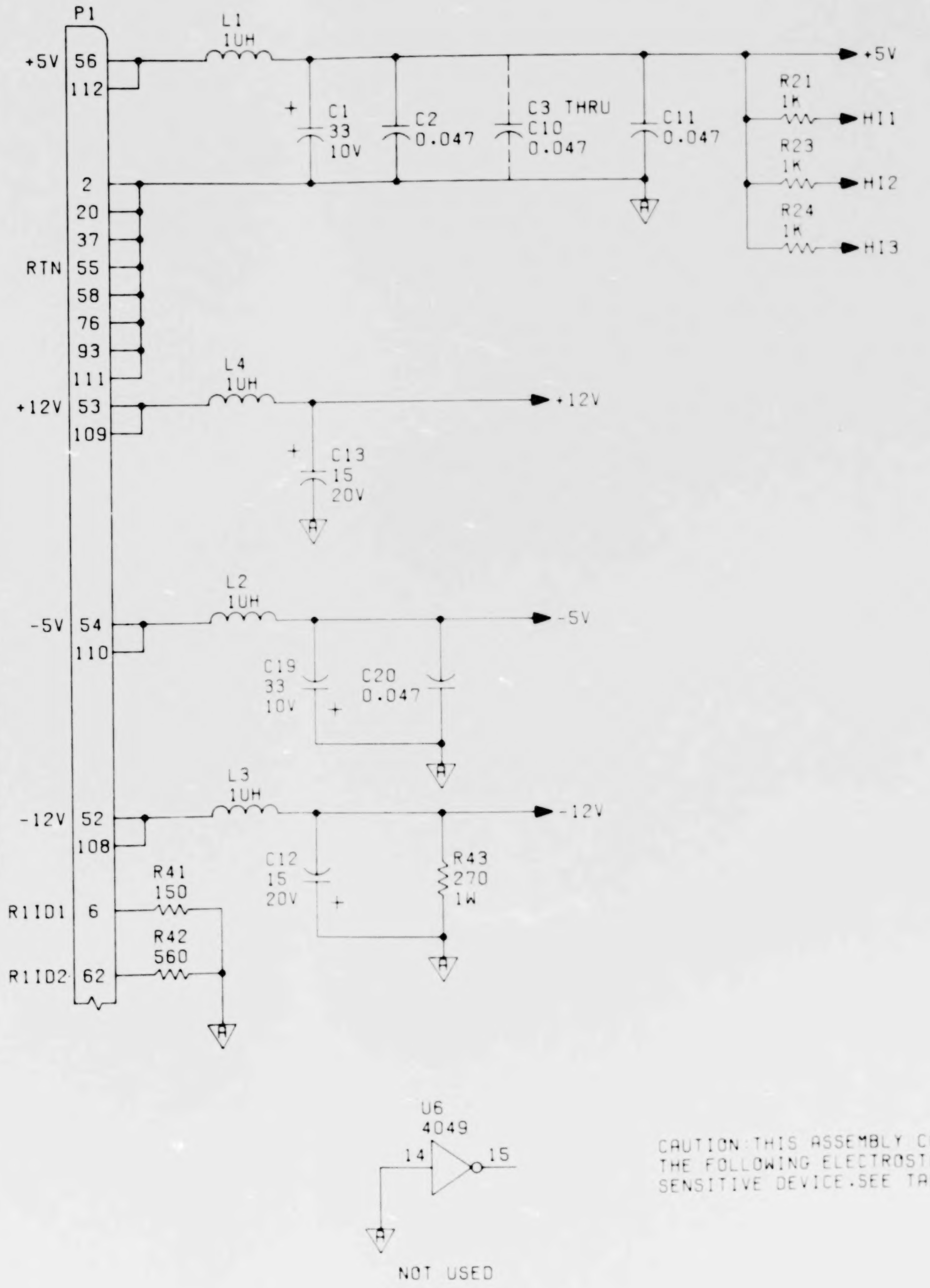


FIG A FIG B

TOP VIEW
NUMBERS ARE FOR REFERENCE ONLY

REV G



CAUTION: THIS ASSEMBLY CONTAINS THE FOLLOWING ELECTROSTATIC SENSITIVE DEVICE. SEE TABLE 1

EL8TH024

Figure FO-7. A5, Receive 1 CCA, Schematic Diagram (Sheet 1 of 7)

best copy available

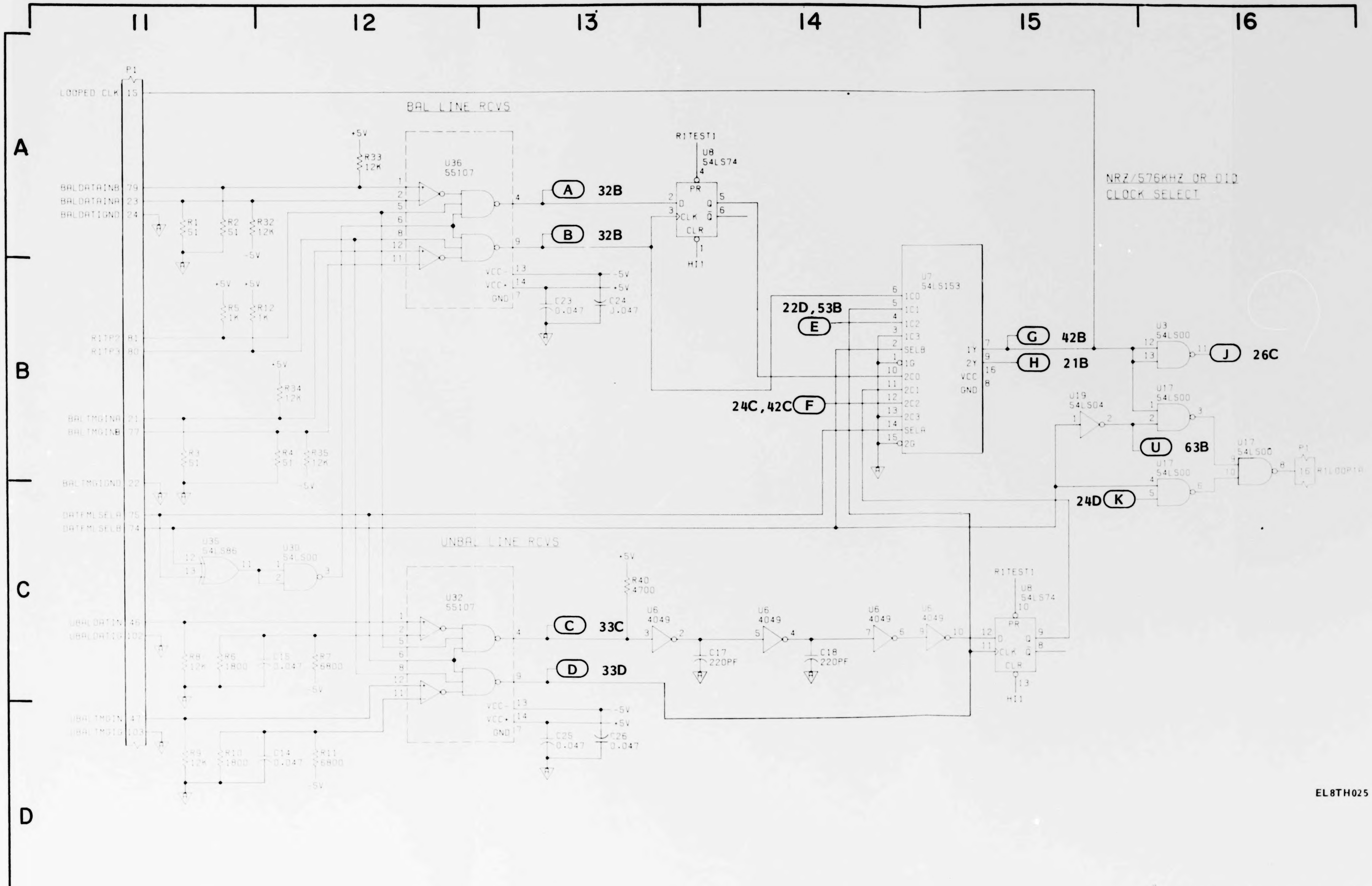


Figure FO-7. A5, Receive 1 CCA, Schematic Diagram (Sheet 2 of 7)

best copy available

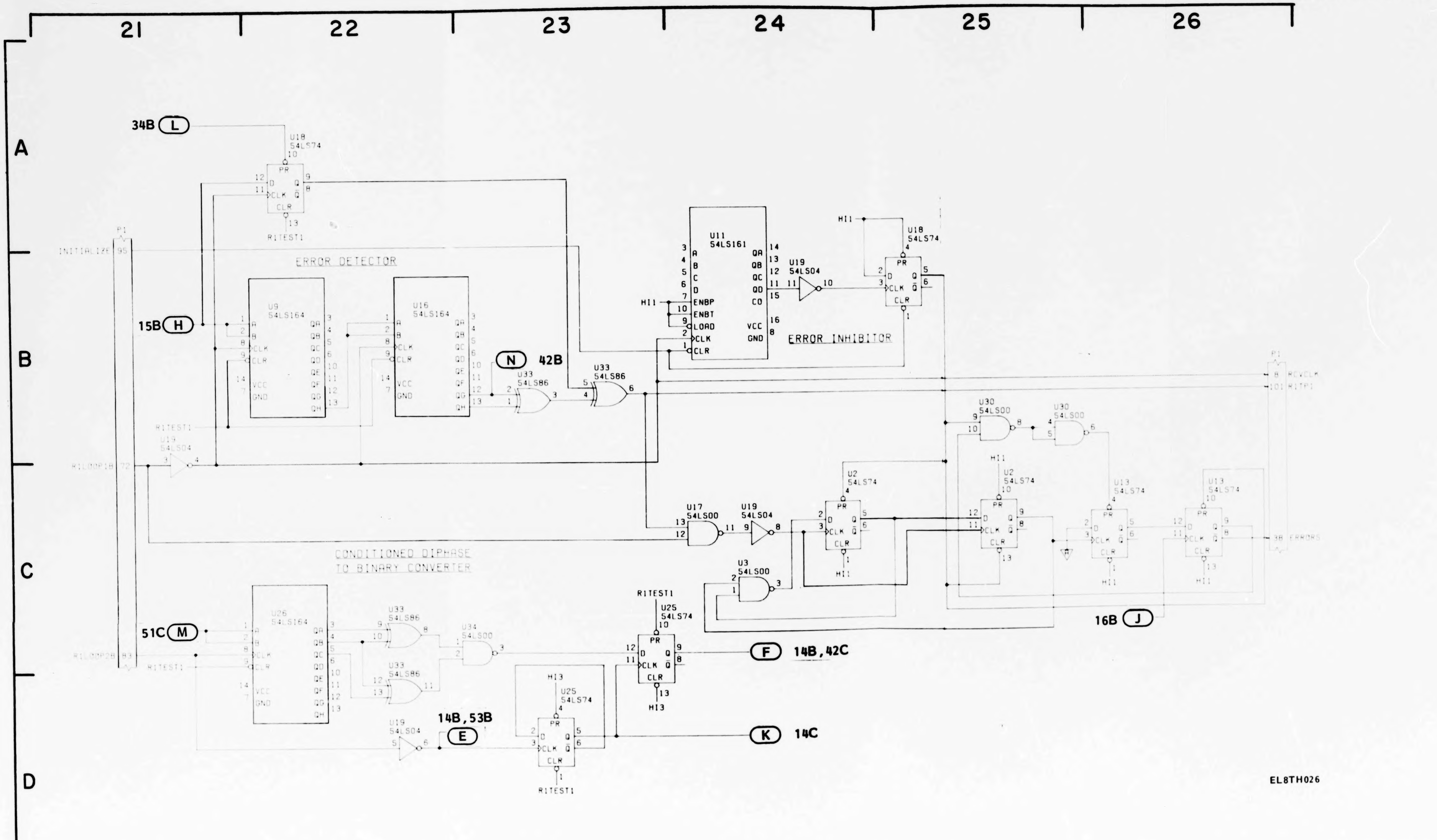


Figure FO-7. A5, Receive 1 CCA, Schematic Diagram (Sheet 3 of 7)

best copy available

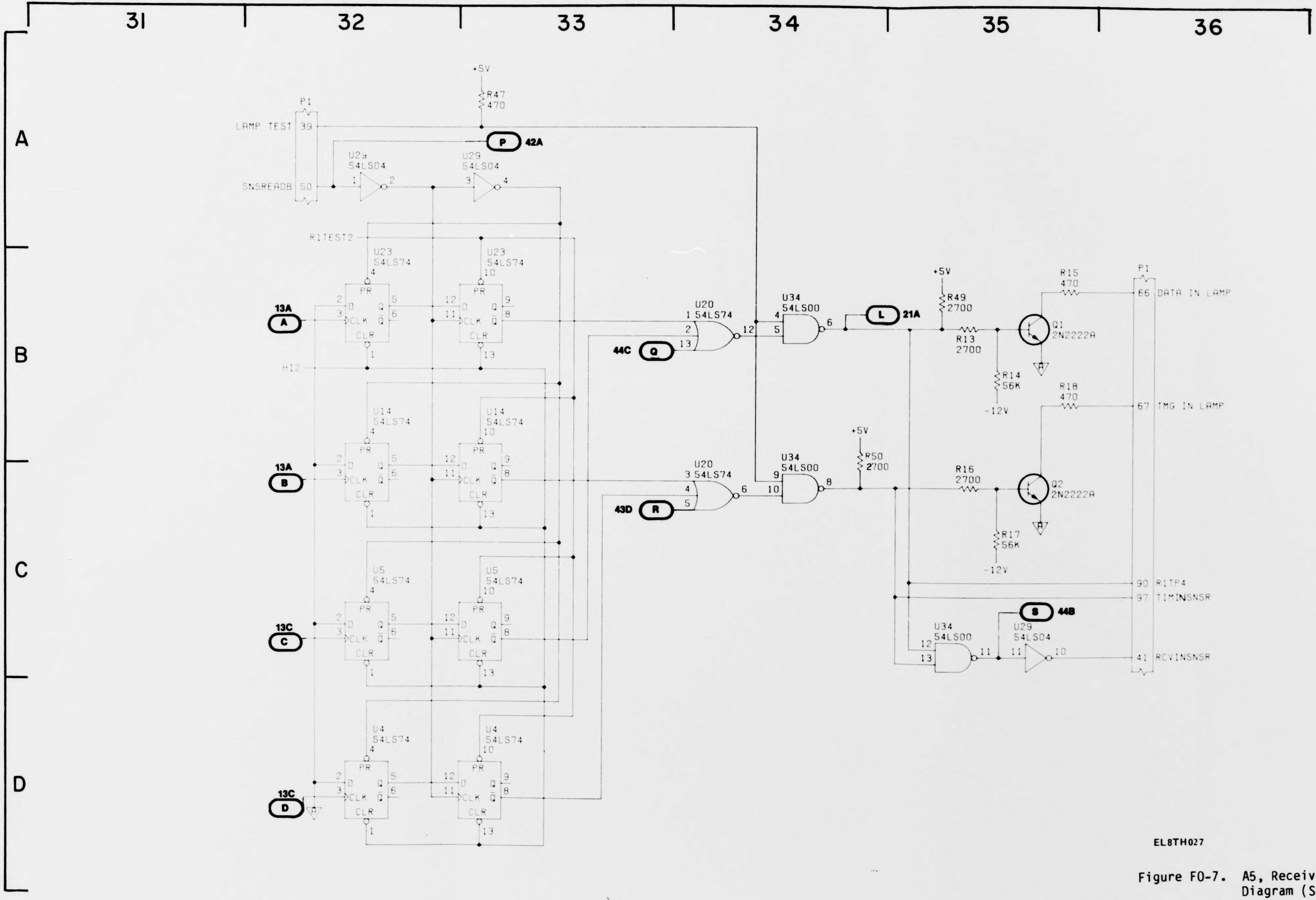


Figure FO-7. A5, Receive 1 CCA, Schematic Diagram (Sheet 4 of 7)

best copy available

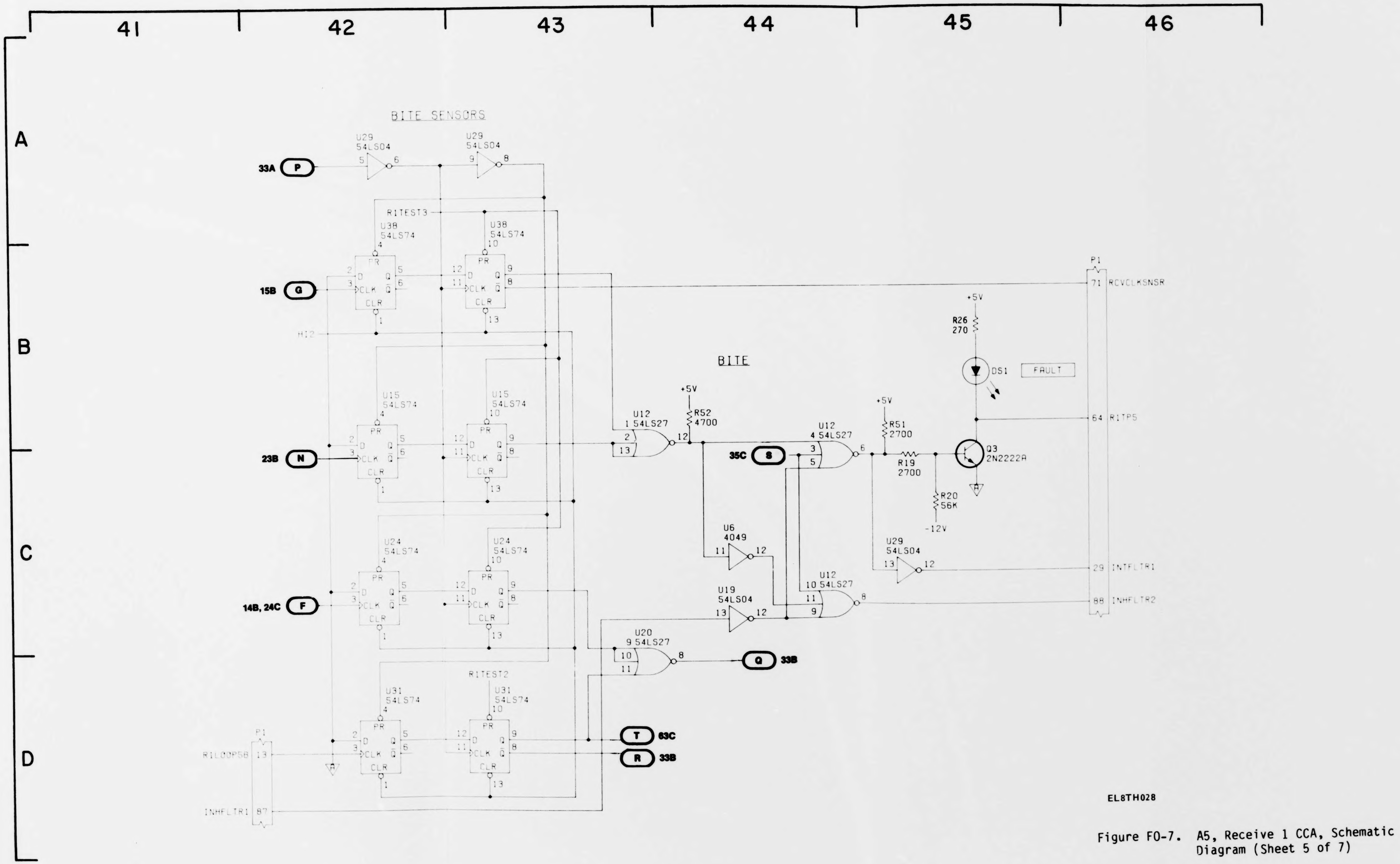


Figure FO-7. A5, Receive 1 CCA, Schematic Diagram (Sheet 5 of 7)

best copy available

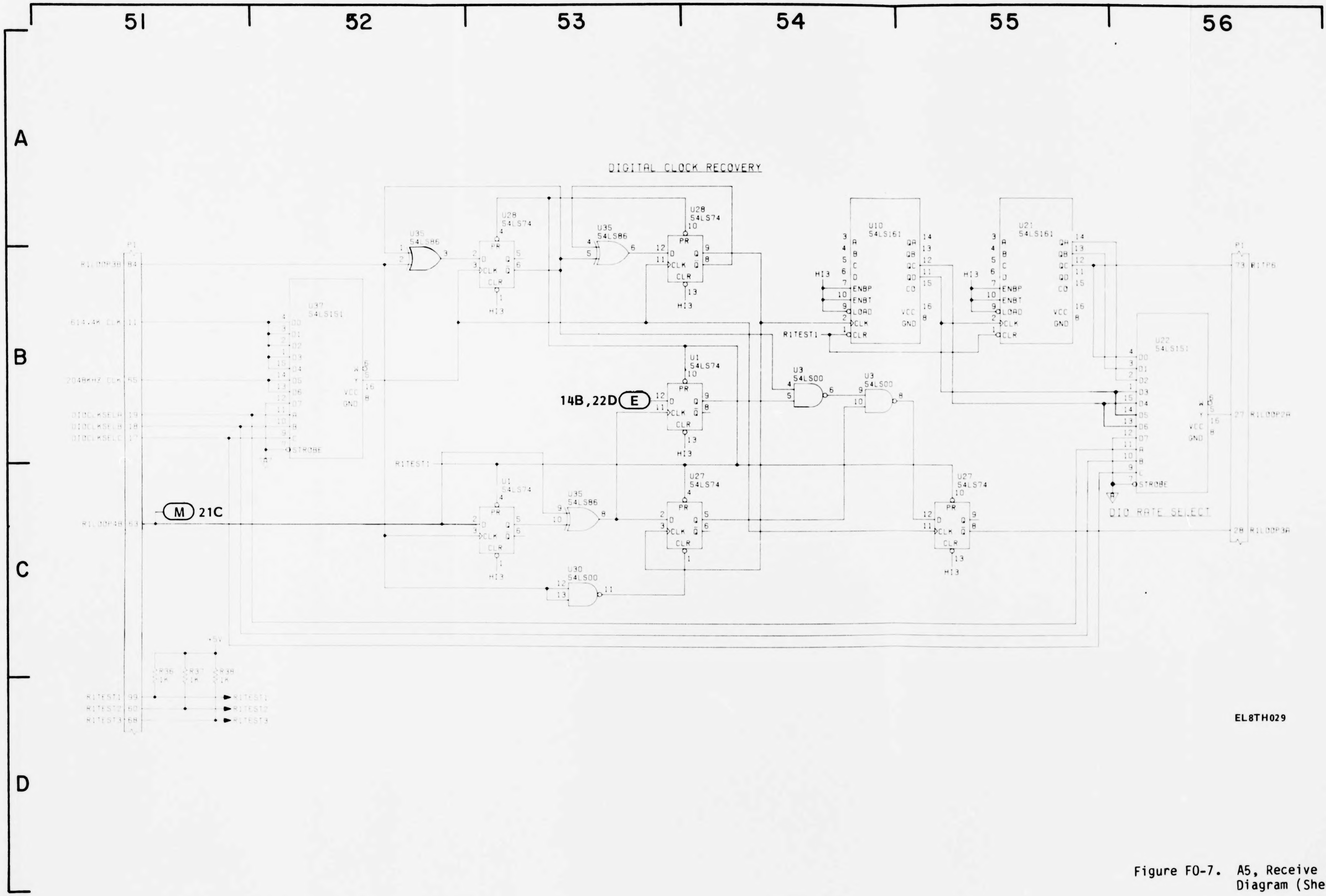


Figure FO-7. A5, Receive 1 CCA, Schematic Diagram (Sheet 6 of 7)

best copy available

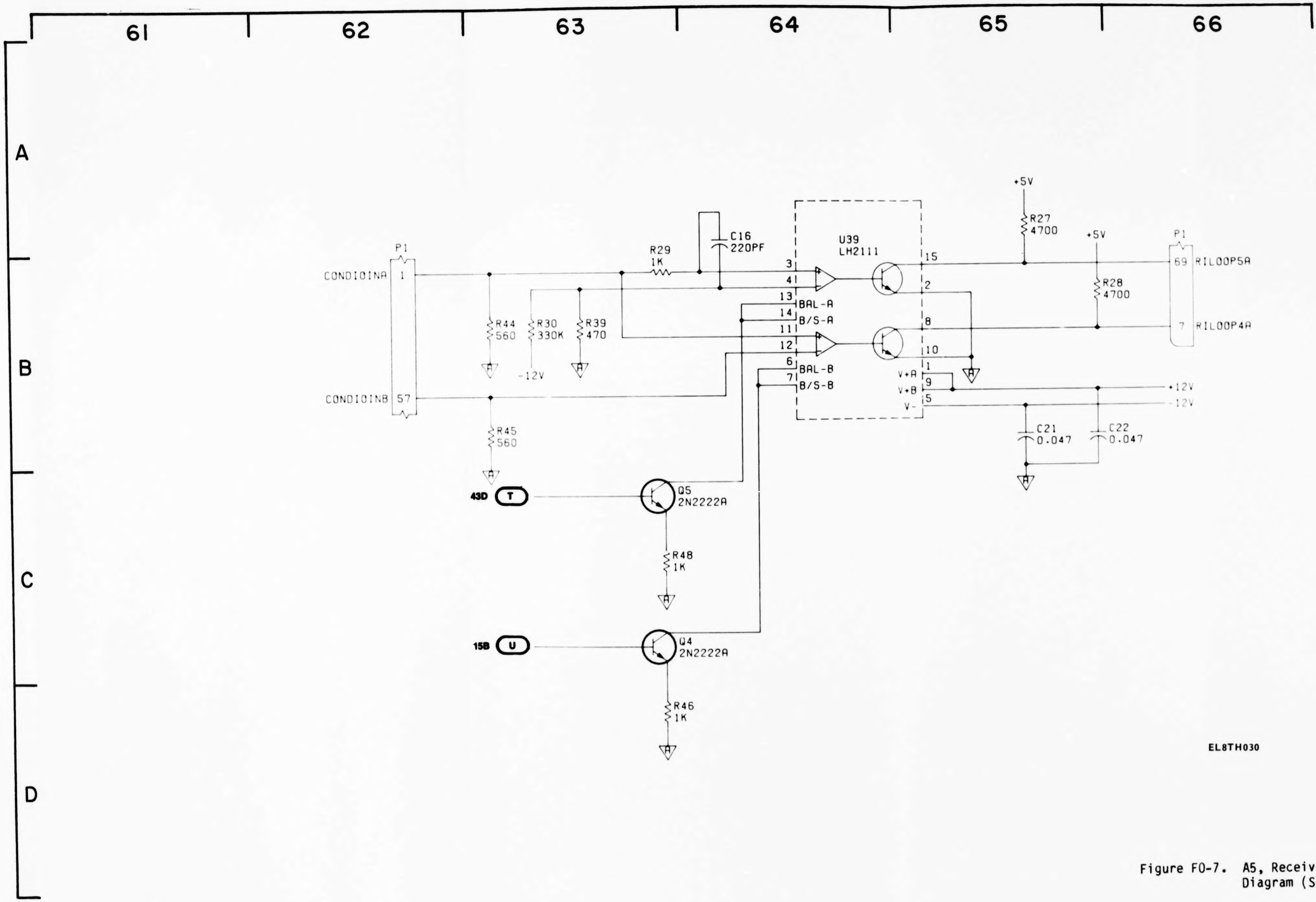


Figure FO-7. A5, Receive 1 CCA, Schematic Diagram (Sheet 7 of 7)

best copy available

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:FOR COMPLETE DESIGNATION.PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE SPECIFIED:
   - A. RESISTANCE VALUES ARE IN OHMS AND ARE 1/4W.±2%
   - B. CAPACITANCE VALUES ARE IN MICROFARADS AND ARE 50V.±10%
   - C. ALL VOLTAGES ARE DC
3. ☐ INDICATES FRONT PANEL MARKING

TABLE 1

REF DES	TYPE	PWR PINS +5V	PWR PINS GND	FIG LTR	ESD
U28.29.31.33	M38510/30001BCX	14	7	A	-
U25.30	M38510/30003BCX	14	7	A	-
U12.18.22.32	M38510/30302BCX	14	7	A	-
U1.4.6.7.9.11. 13.15.19.23.24	M38510/30102BCX	14	7	A	-
U5	M38510/30502BCX	14	7	A	-
U20.21	M38510/30902BEX	16	8	B	-
U2.3.8.10.14. 16.17.26.27	M38510/31503BEX	16	8	B	-
U34	M38510/05503BEX	1	8	A	-

TABLE 2

REF DES HIGHEST USED	REF DES NOT USED
C13	
CR2	
DS1	
L2	
P1	
Q4	
R38	R1
U34	
VR1	

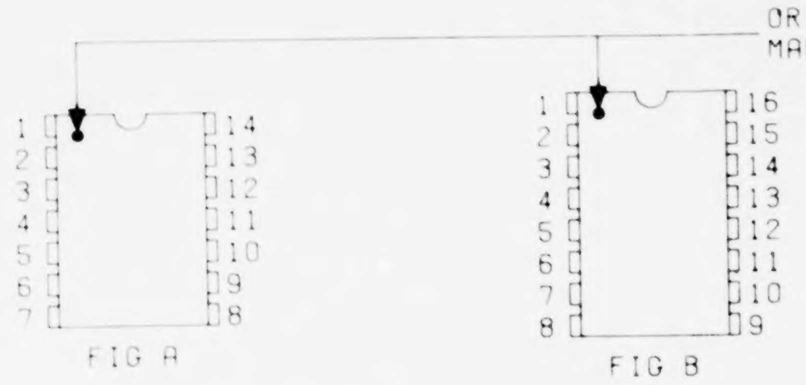
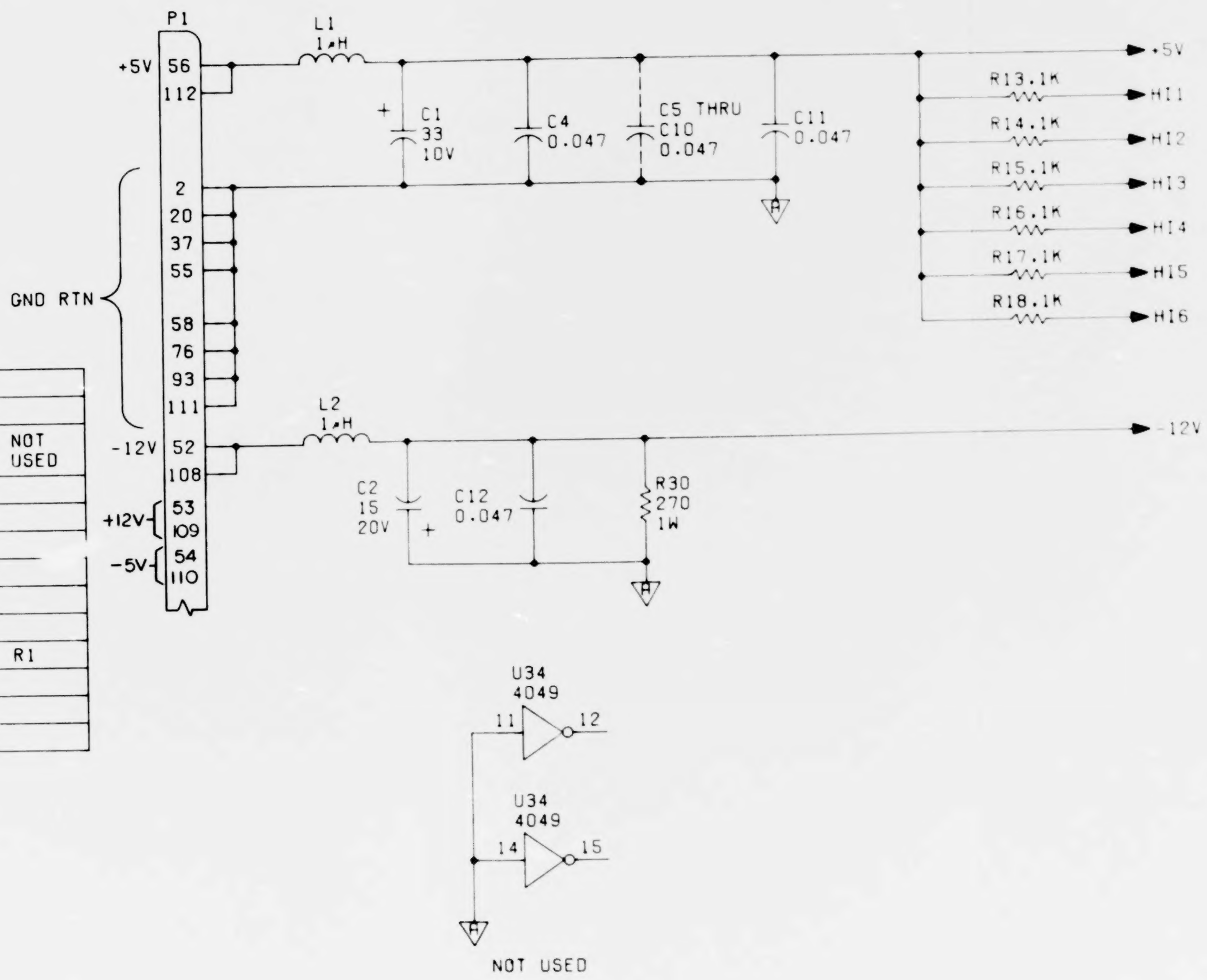


FIG A

FIG B

TOP VIEW
NUMBERS ARE FOR REFERENCE ONLY

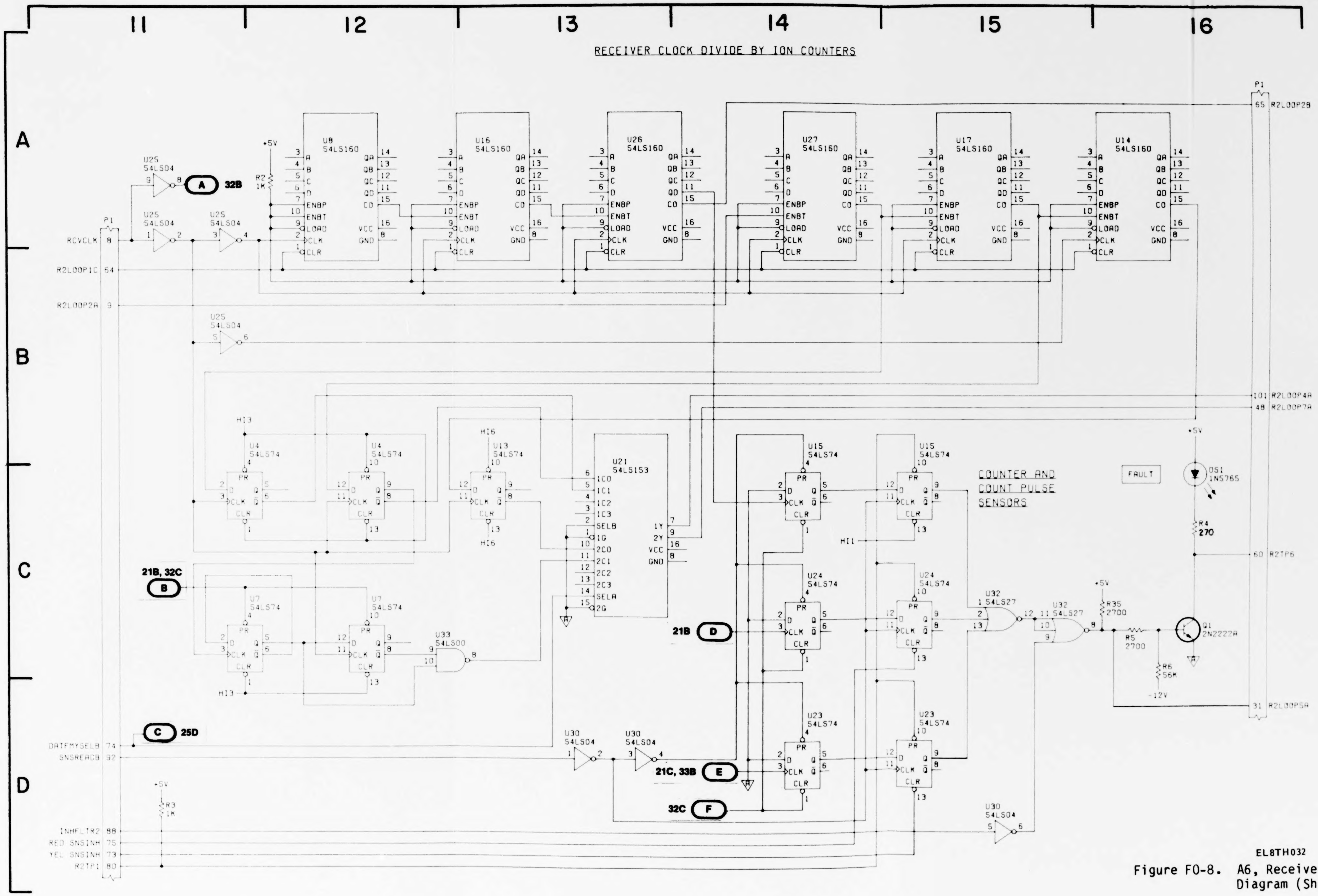


REV L

EL8TH031

Figure FO-8. A6, Receive 2 CCA, Schematic Diagram (Sheet 1 of 4)

best copy available



EL8TH032

Figure FO-8. A6, Receive 2 CCA, Schematic Diagram (Sheet 2 of 4)

best copy available

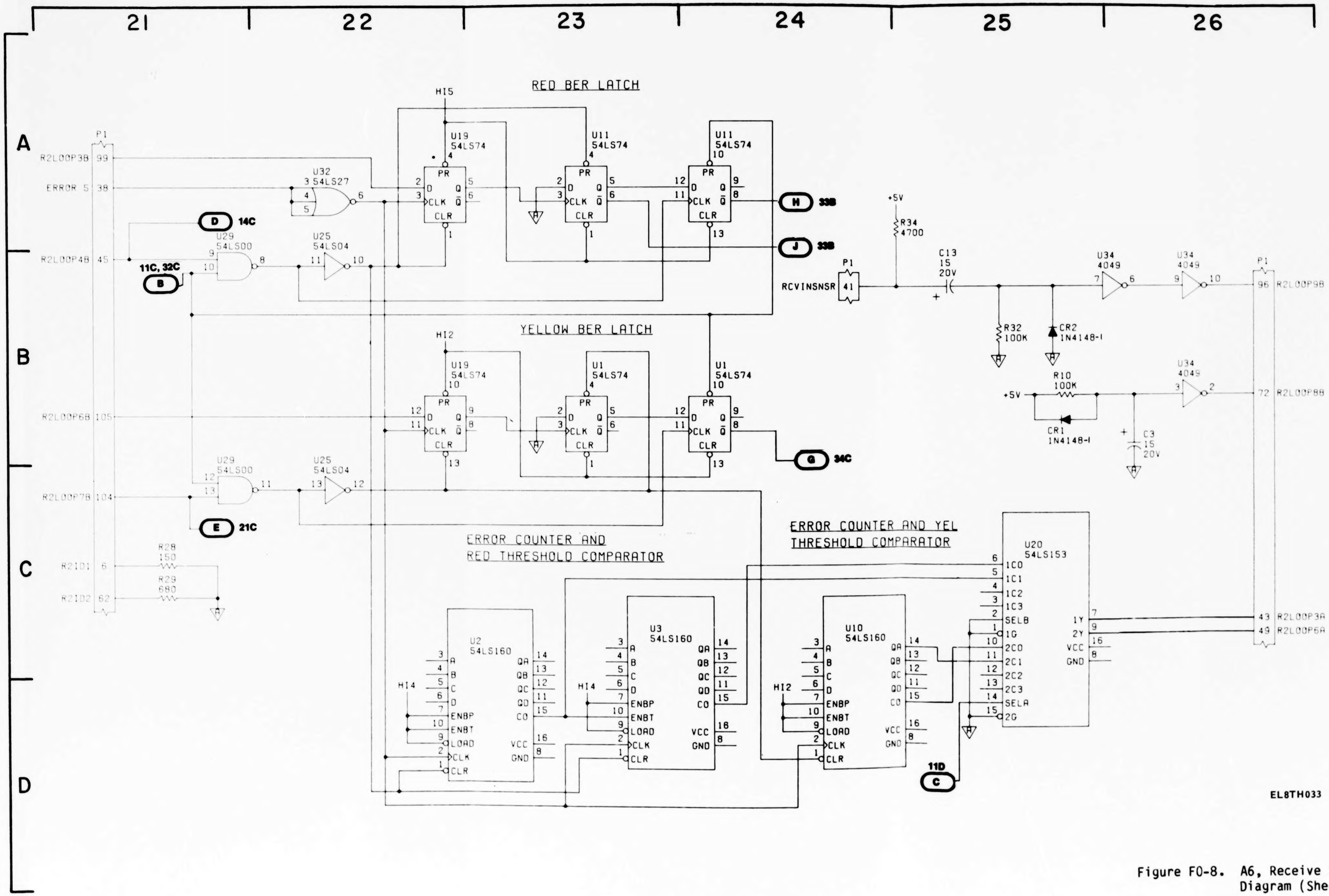


Figure FO-8. A6, Receive 2 CCA, Schematic Diagram (Sheet 3 of 4)

best copy available

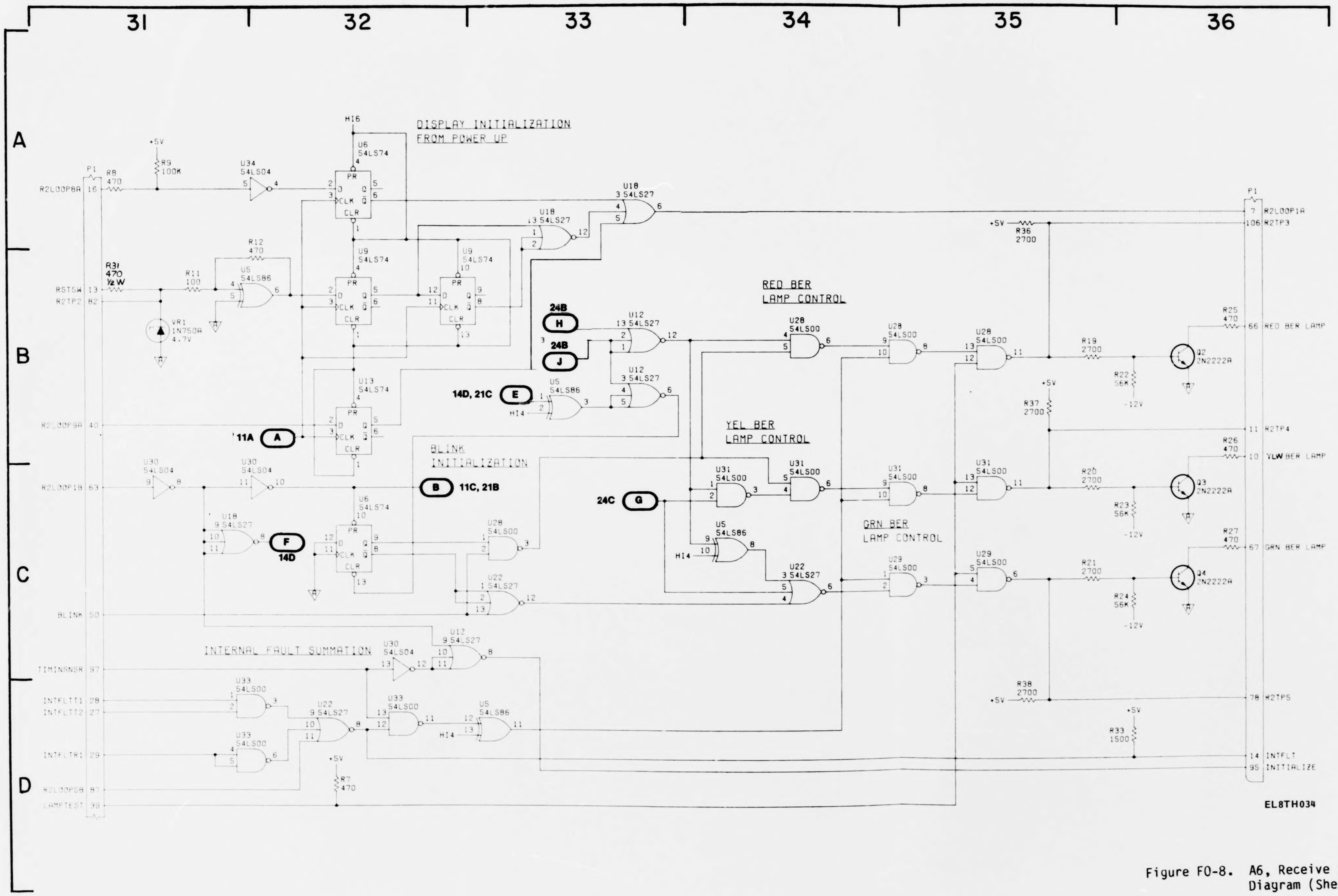
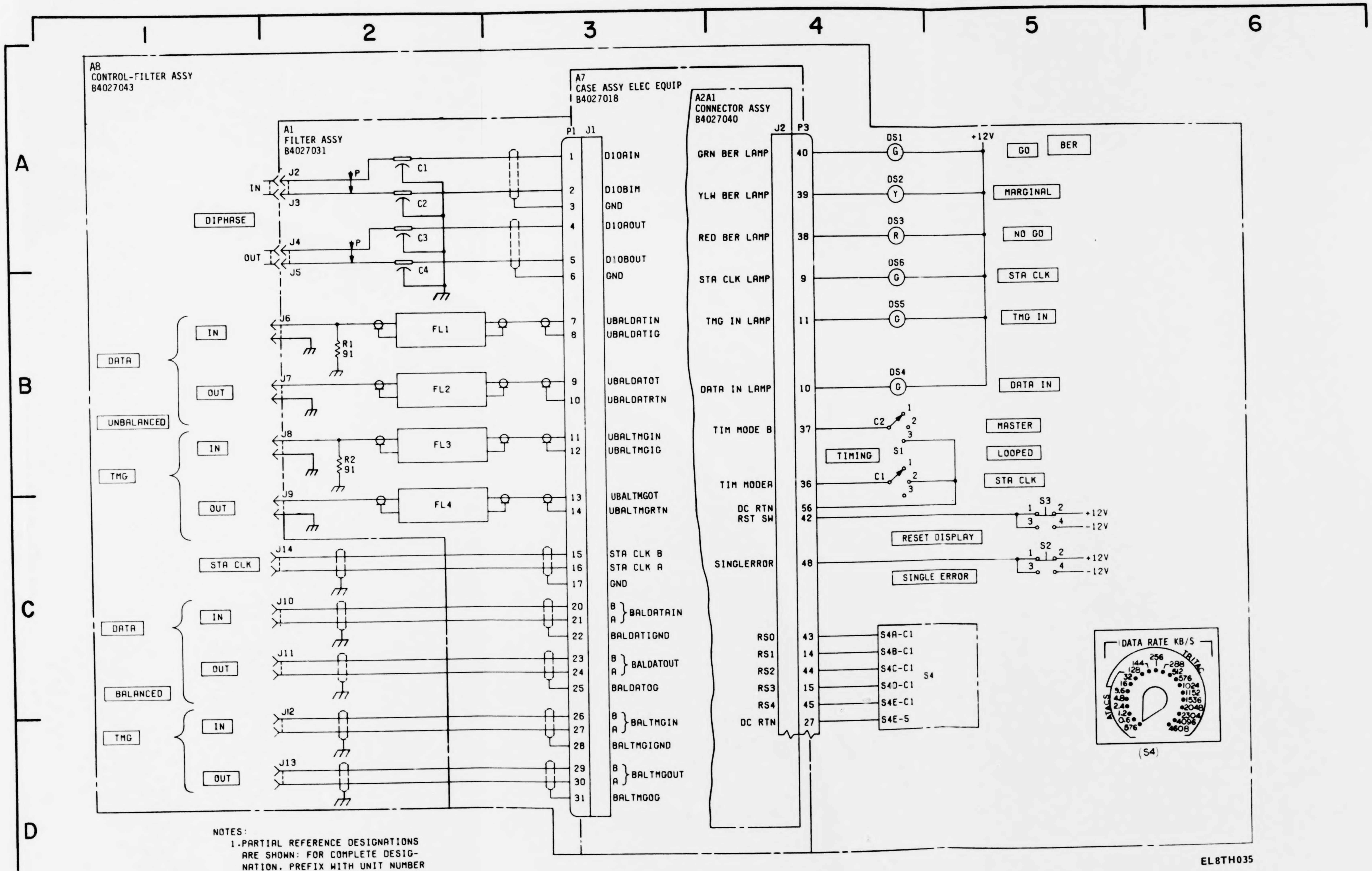


Figure FO-8. A6, Receive 2 CCA, Schematic Diagram (Sheet 4 of 4)

best copy available



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION, PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION(S)
2. UNLESS OTHERWISE SPECIFIED
   A. RESISTANCE VALUES ARE IN OHMS
   B. CAPACITANCE VALUES ARE IN MICROFARADS
   C. ALL VOLTAGES ARE DC

REV C

Figure FO-9. A8, Control Filter Assembly, Schematic Diagram (Sheet 1 of 2)

best copy available

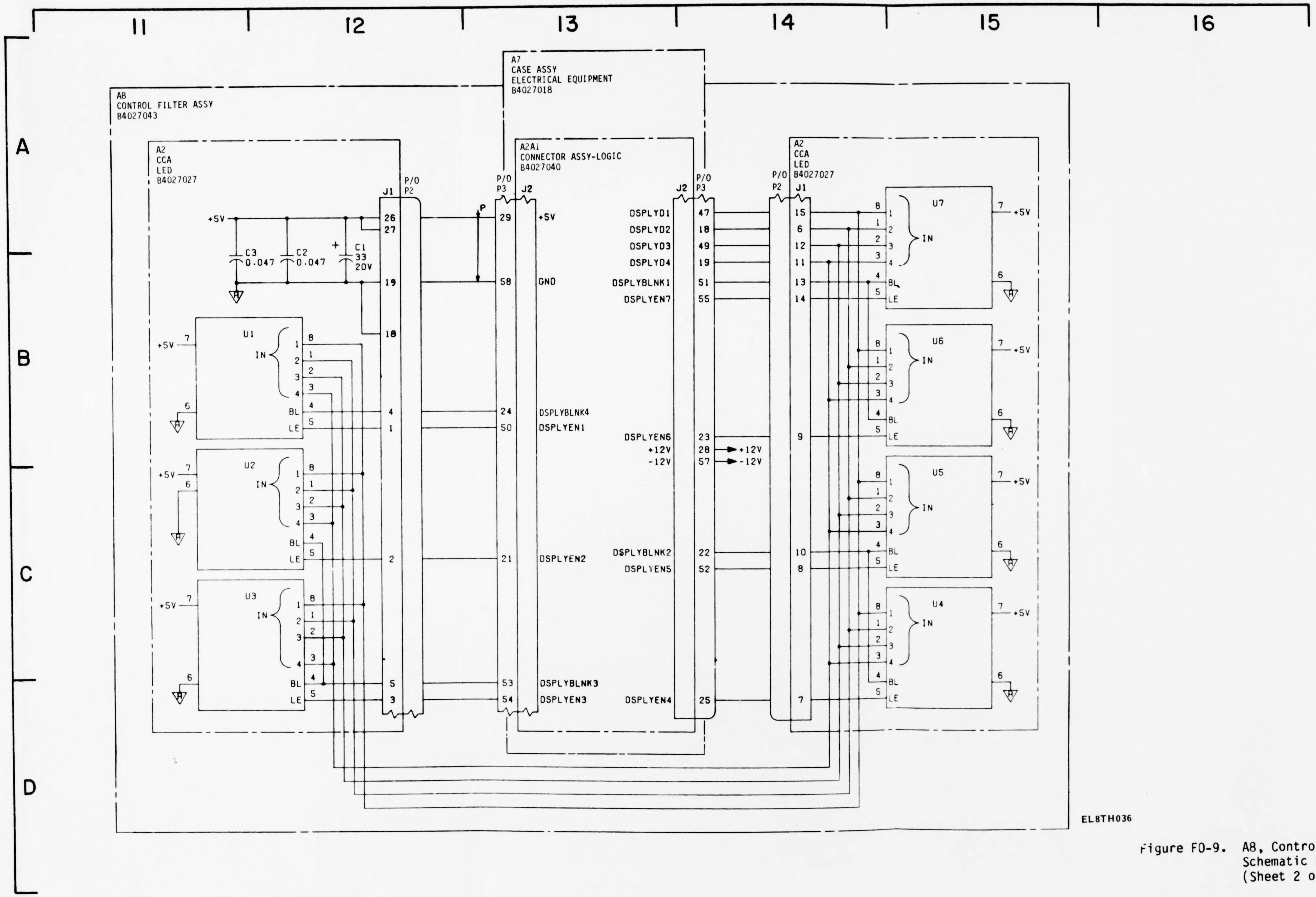


Figure FO-9. A8, Control Filter Assembly, Schematic Diagram (Sheet 2 of 2)

best copy available

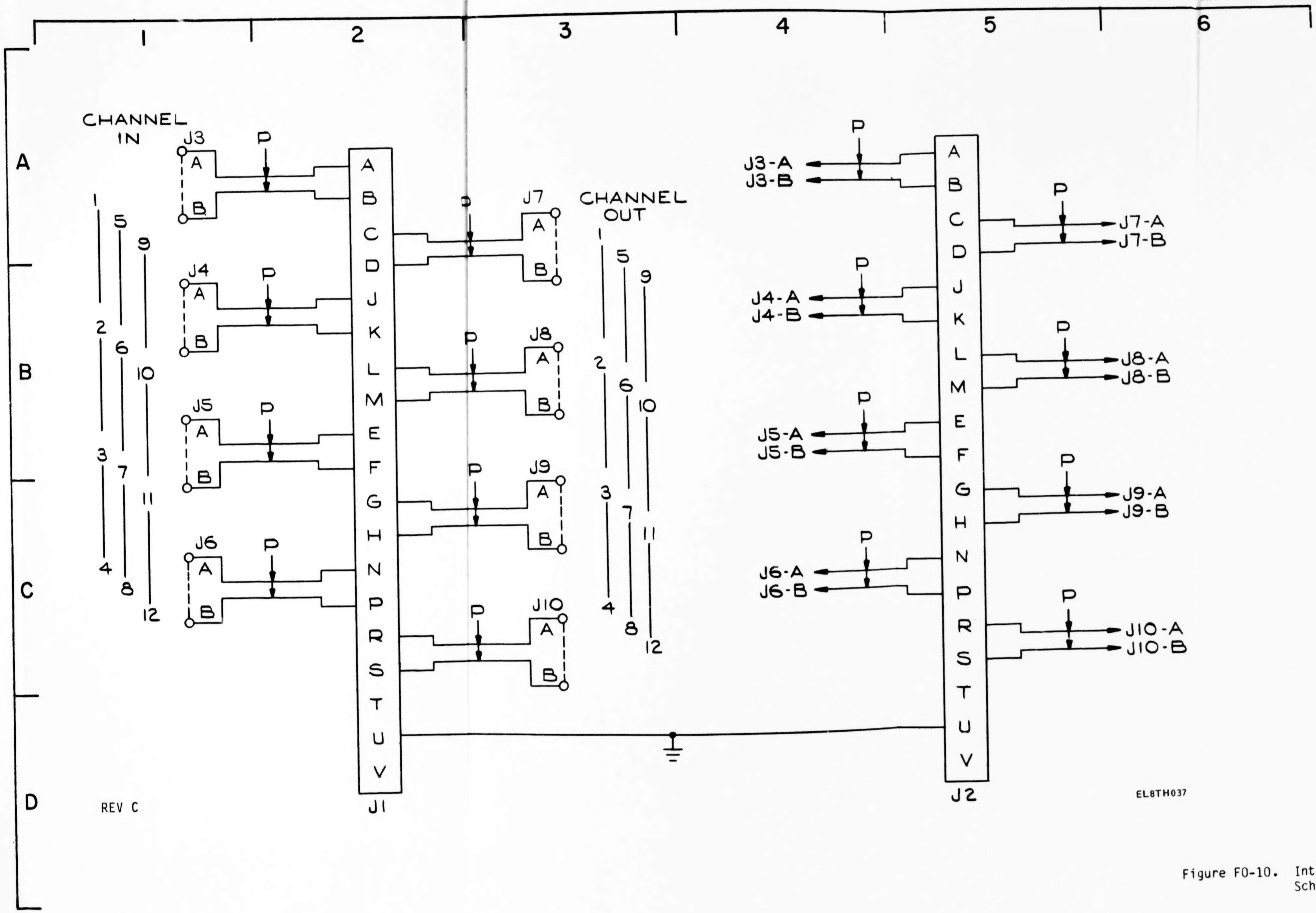


Figure FO-10. Interface Box Assembly Schematic Diagram

best copy available